

FIG. 1

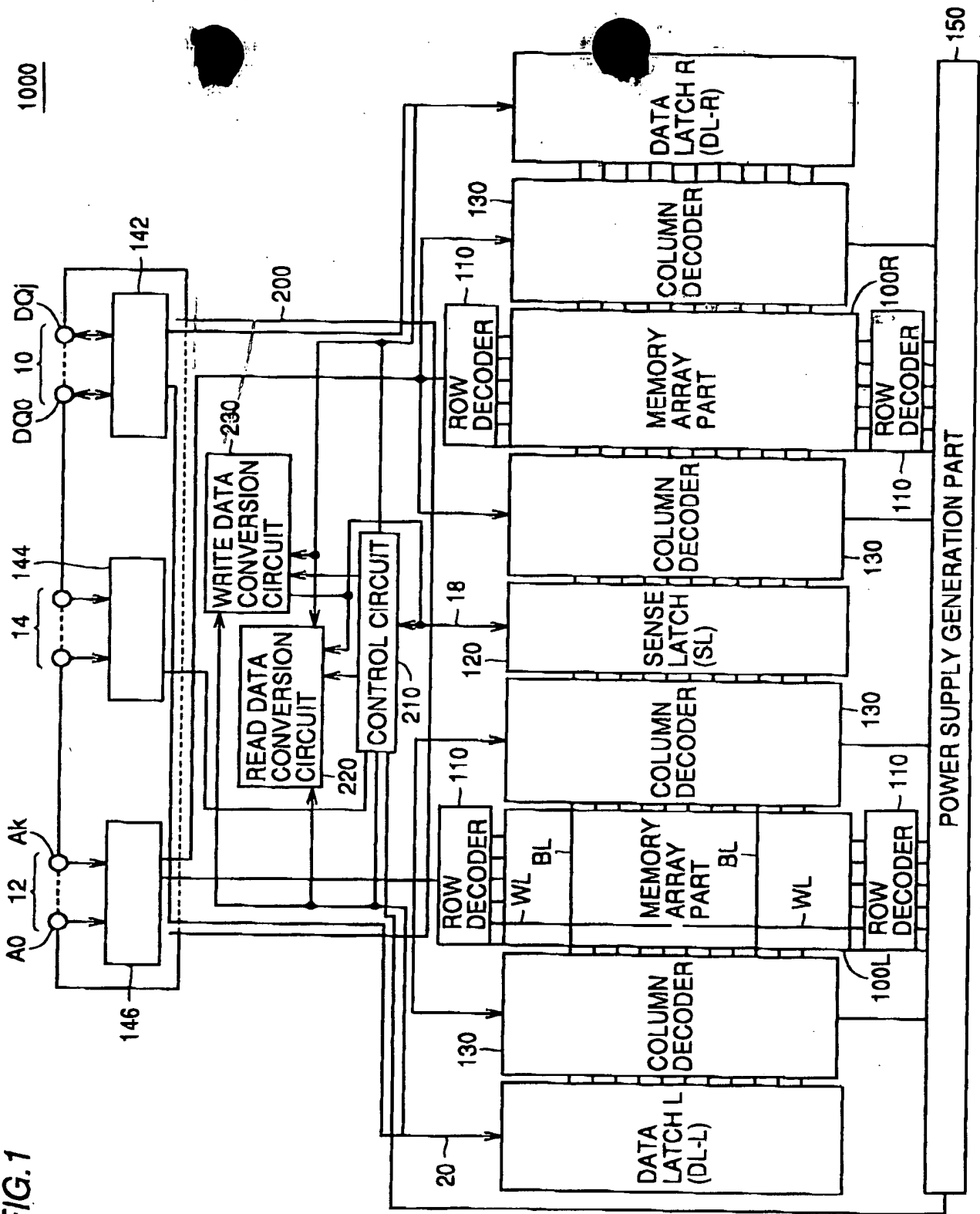


FIG.2

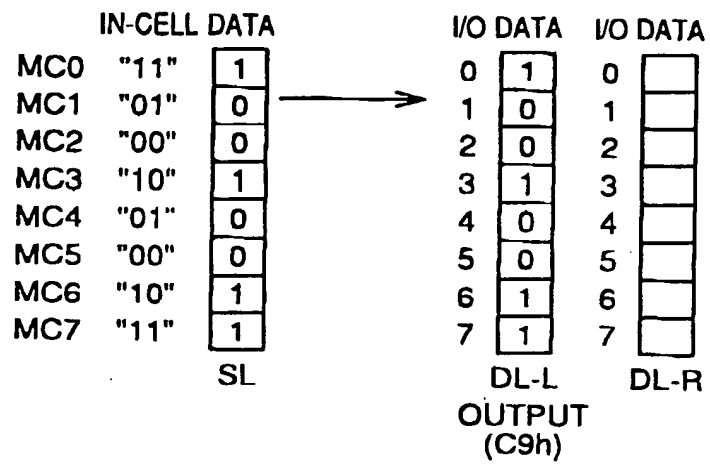


FIG.3

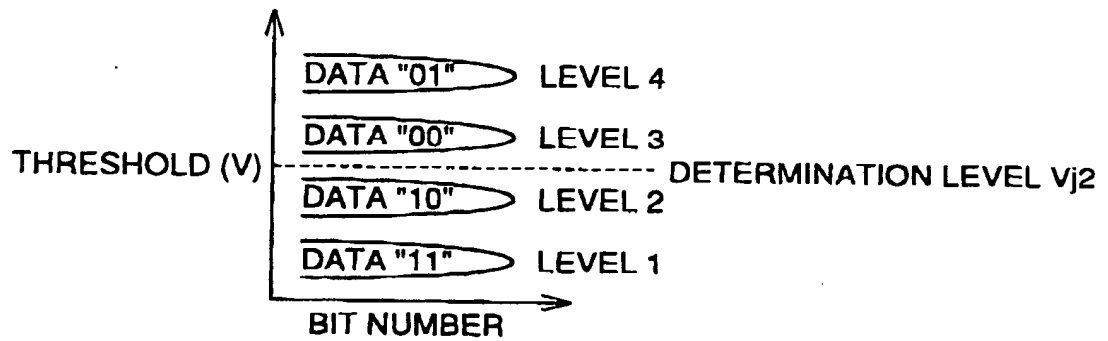


FIG.4

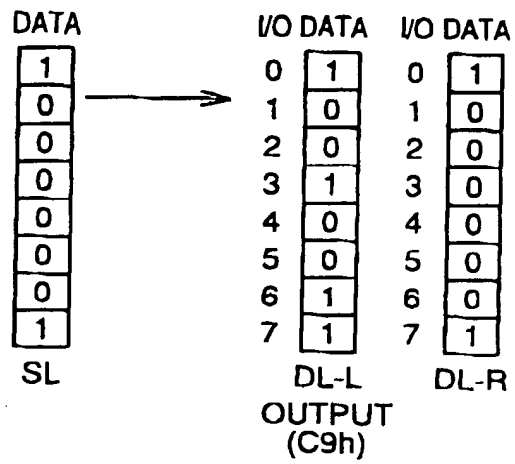


FIG.5

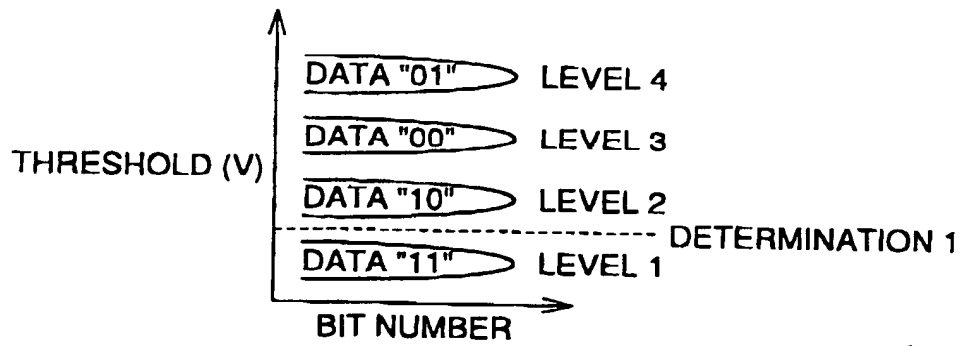


FIG.6

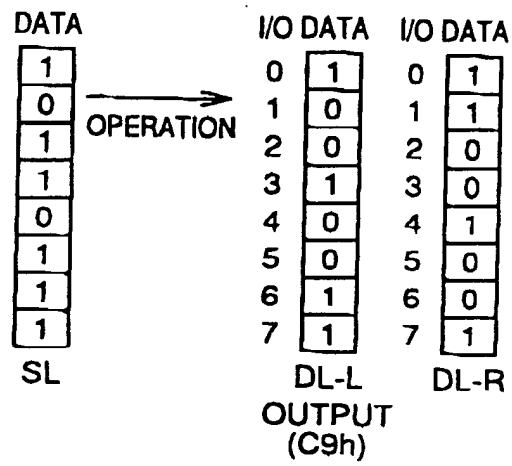


FIG.7

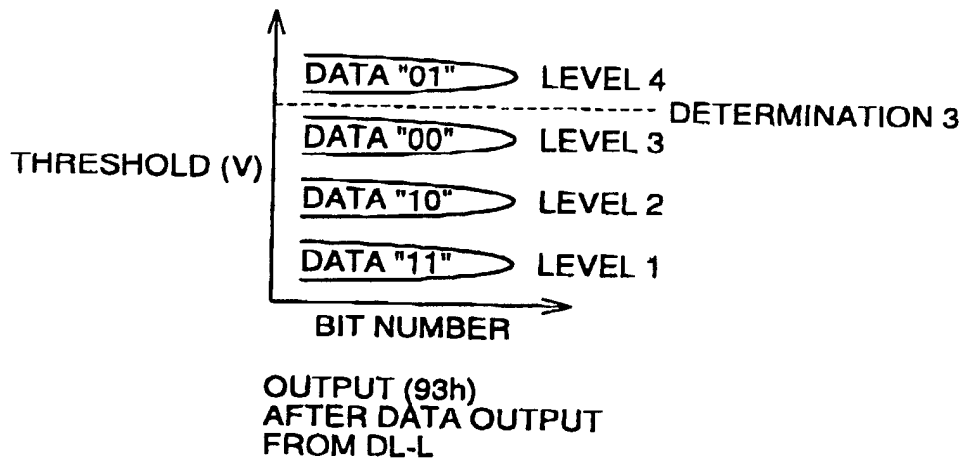


FIG. 8

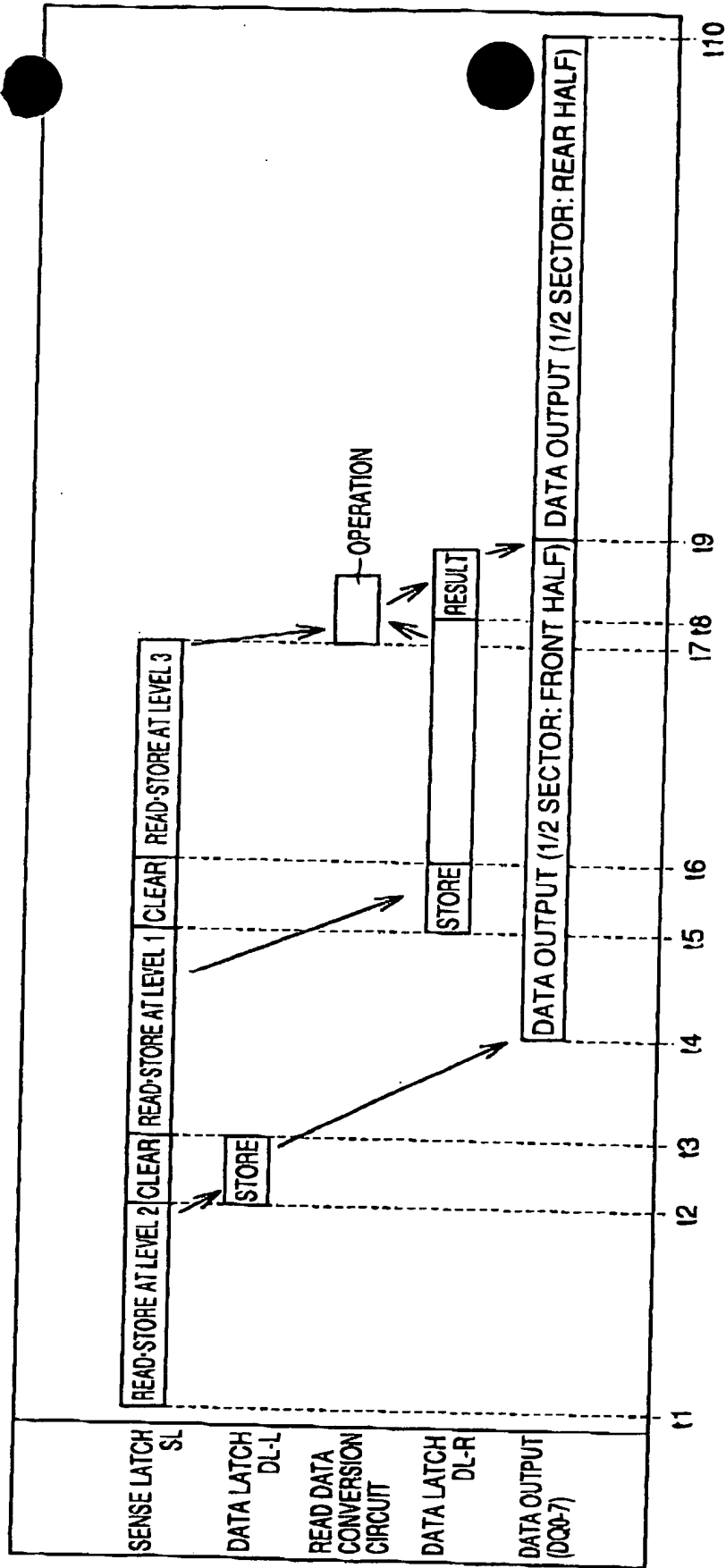


FIG.9

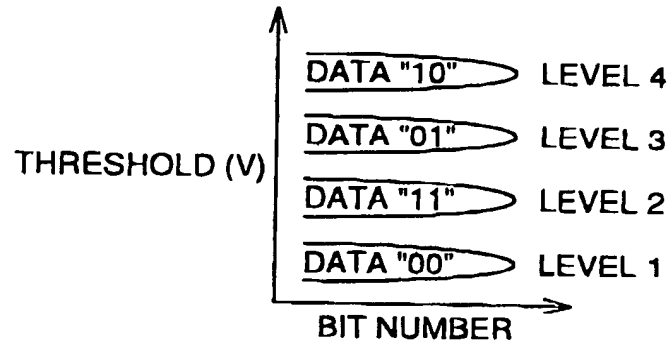


FIG.10

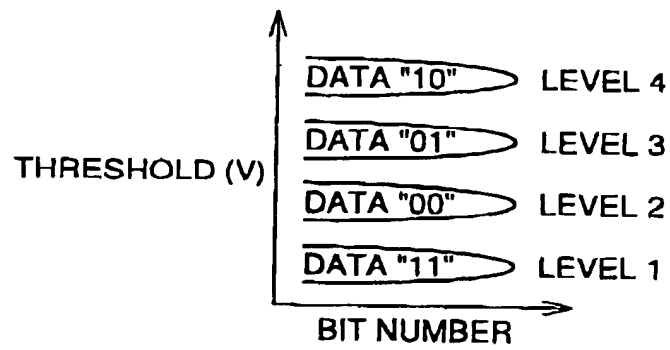


FIG. 11

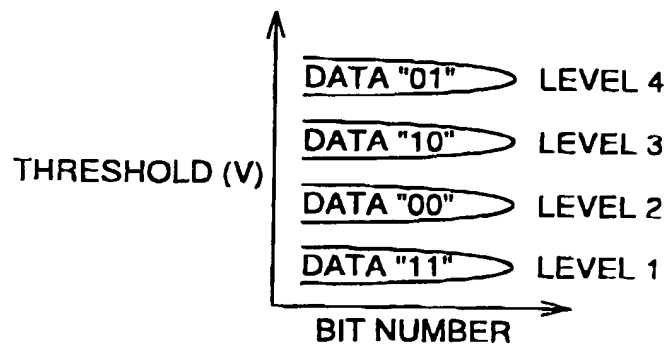


FIG. 12

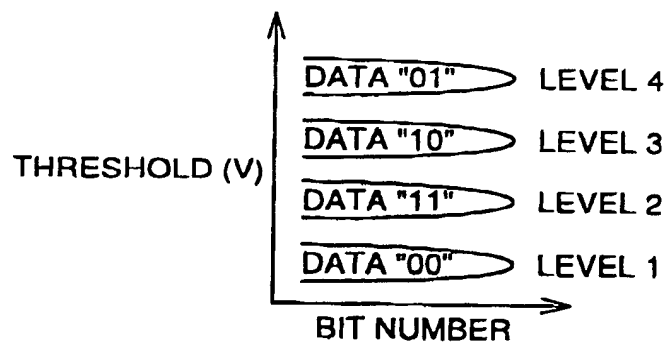


FIG. 13

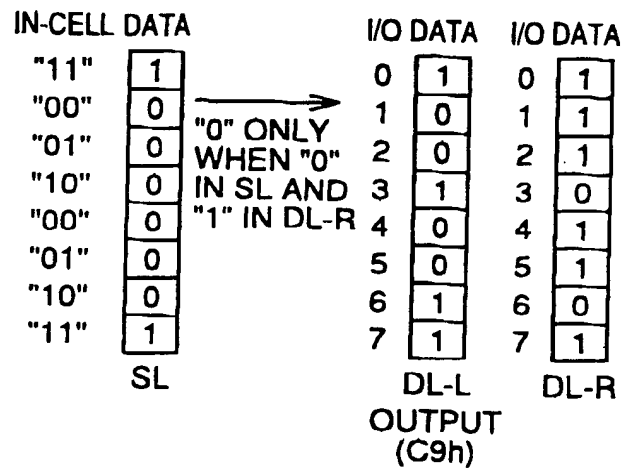
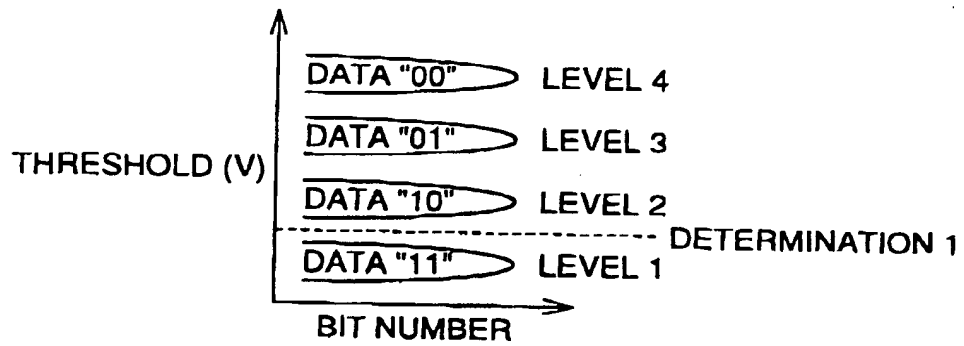


FIG. 14



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FIG. 15

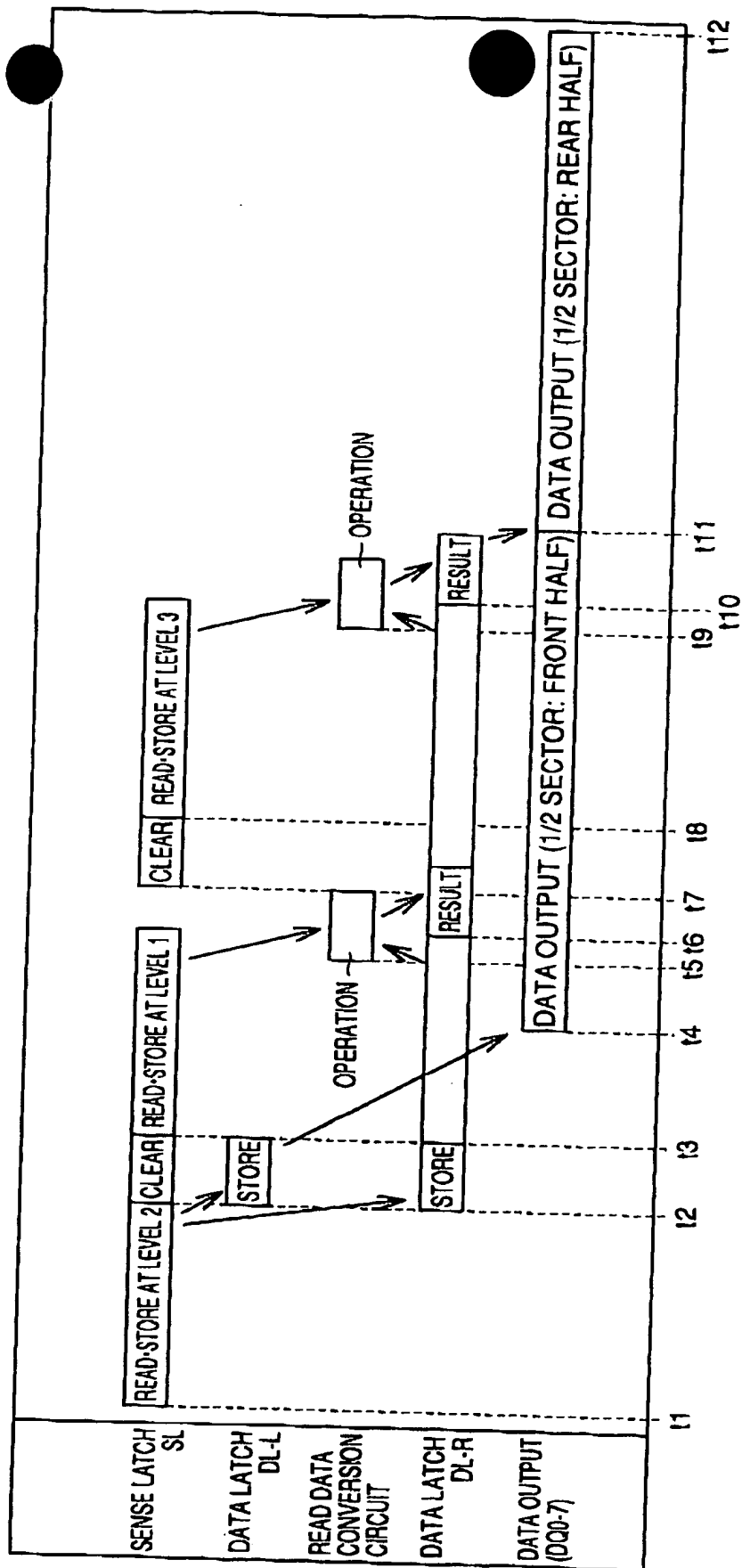


FIG. 16A

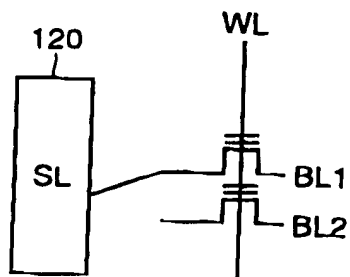


FIG. 16B

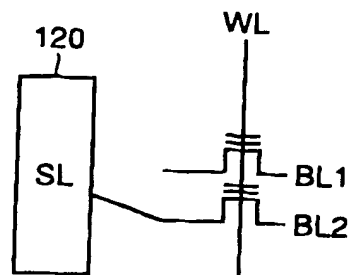


FIG. 17

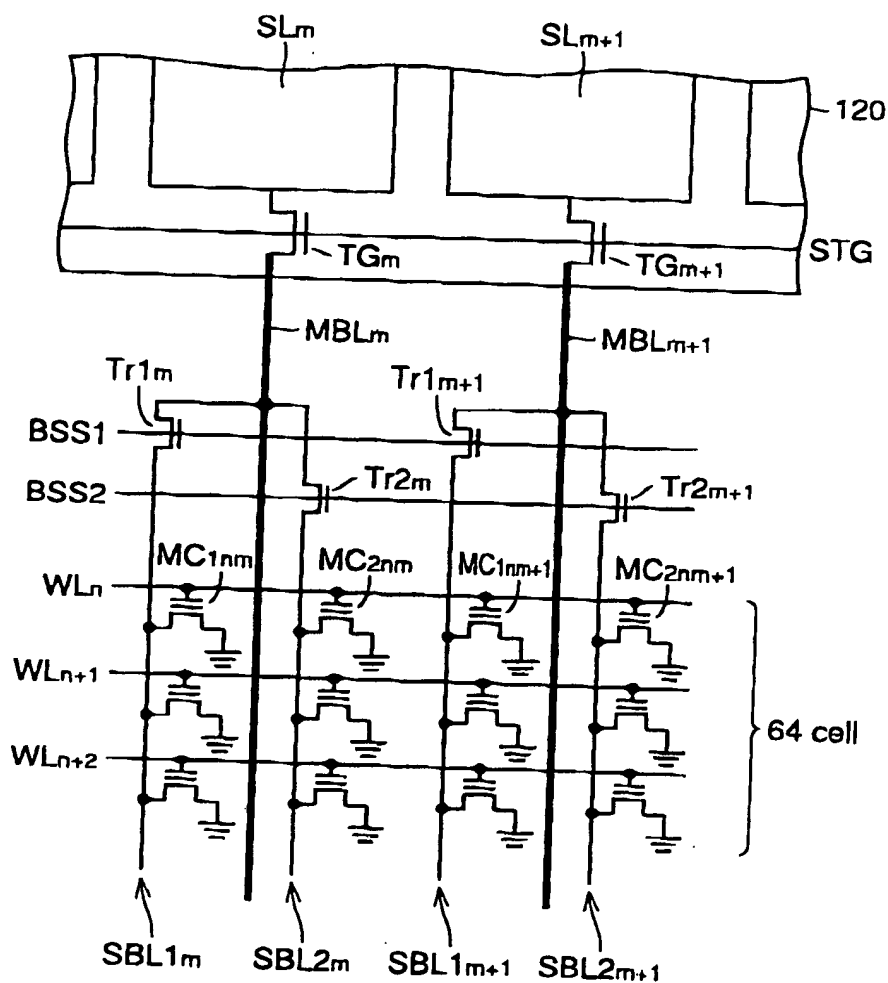


FIG. 18

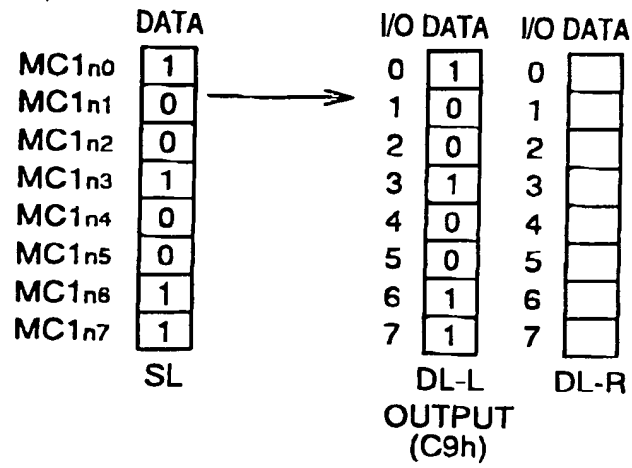


FIG. 19

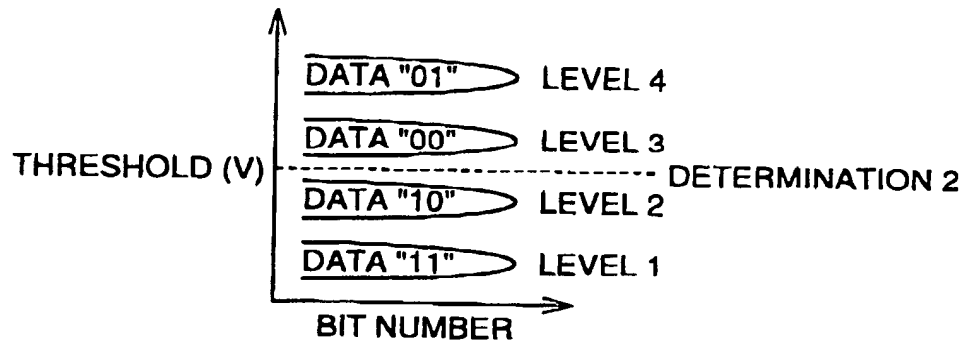


FIG.20

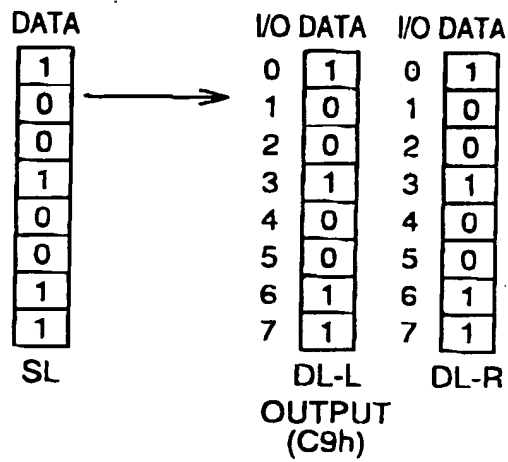


FIG.21

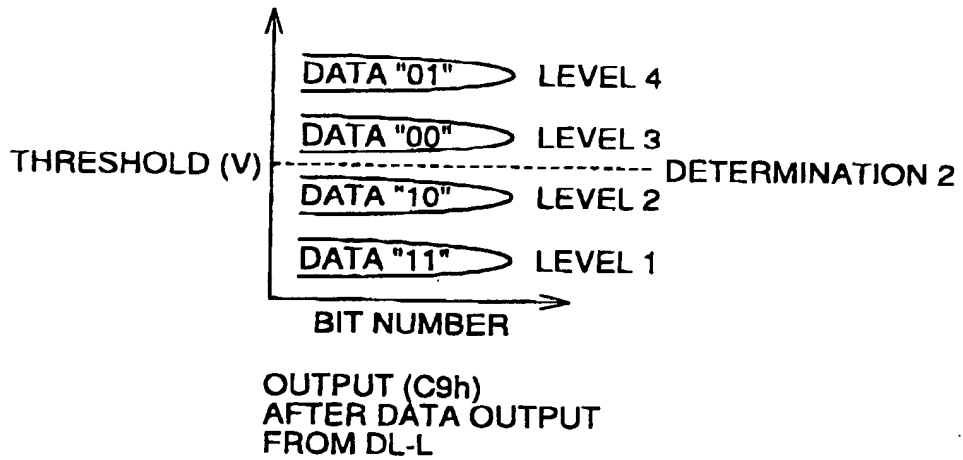


FIG.22

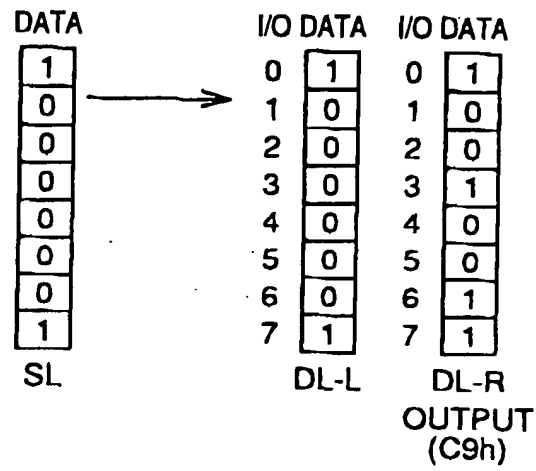


FIG.23

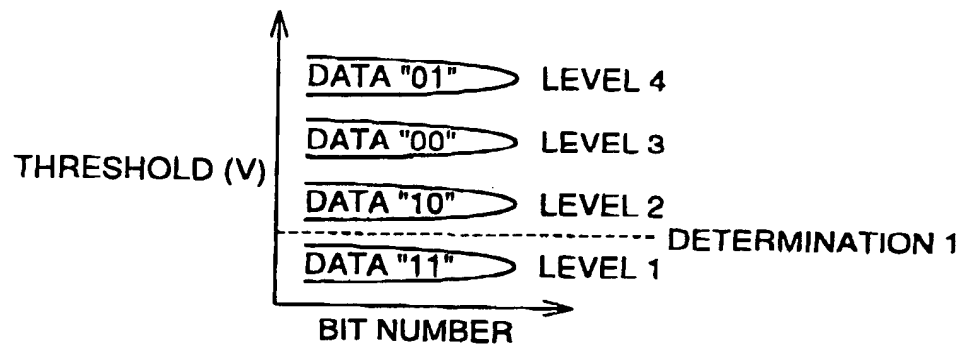


FIG.24

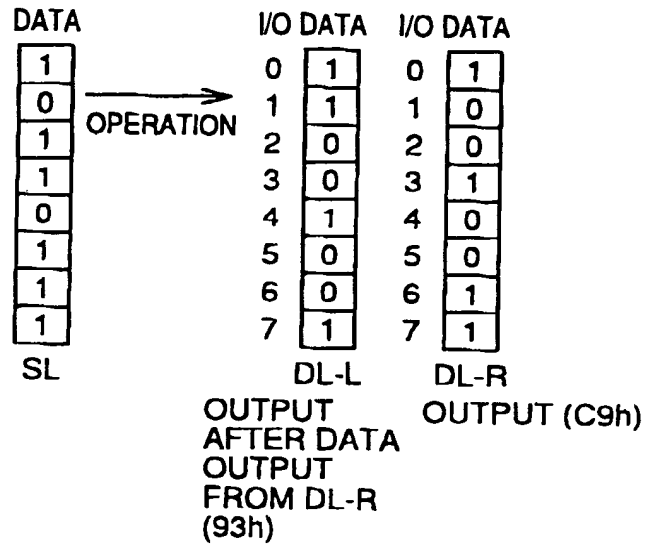


FIG.25

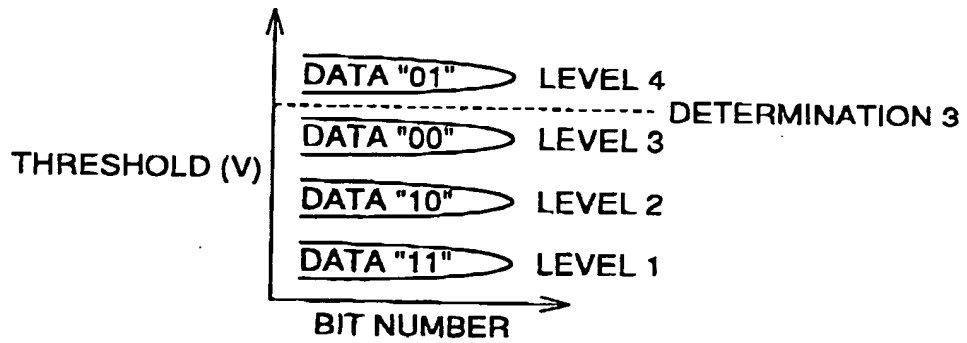


FIG.26

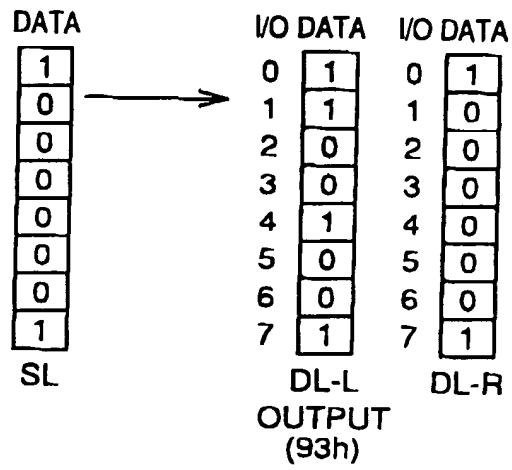


FIG.27

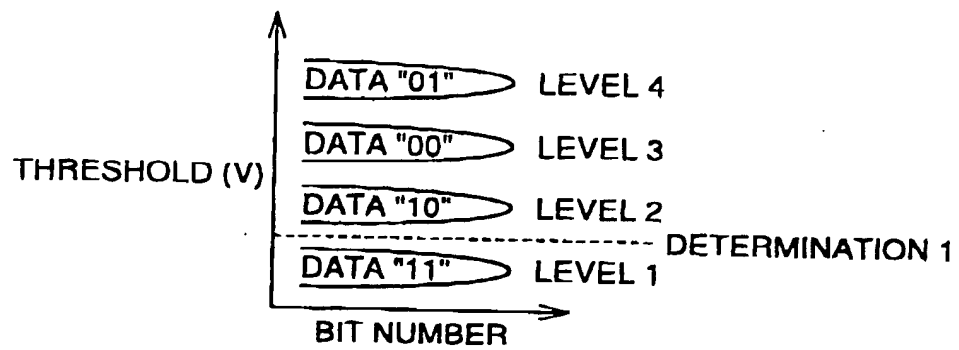


FIG.28

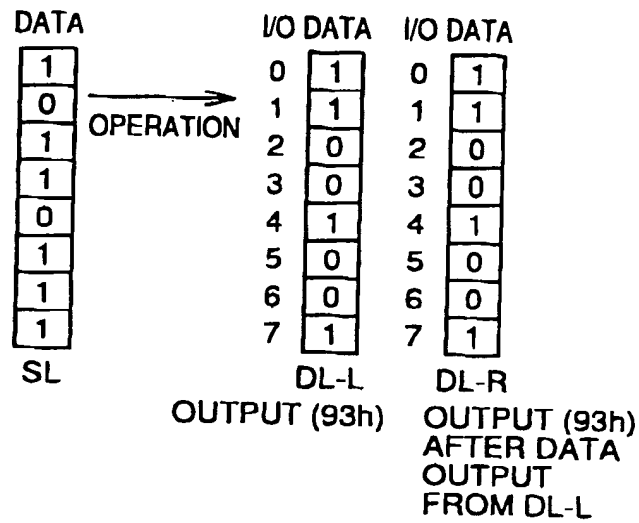


FIG.29

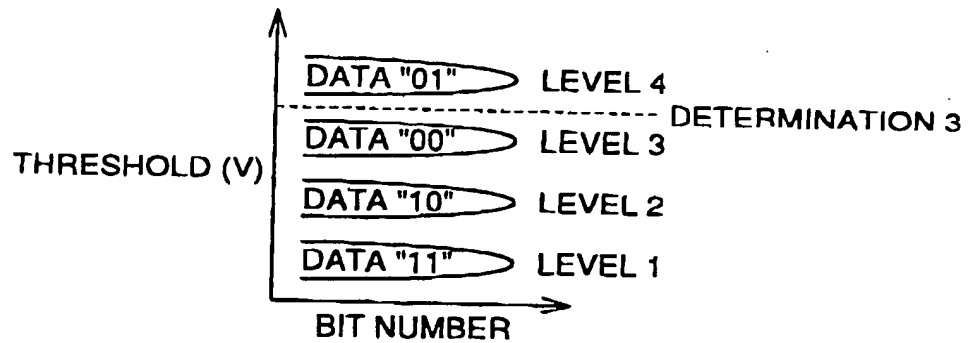


FIG.30

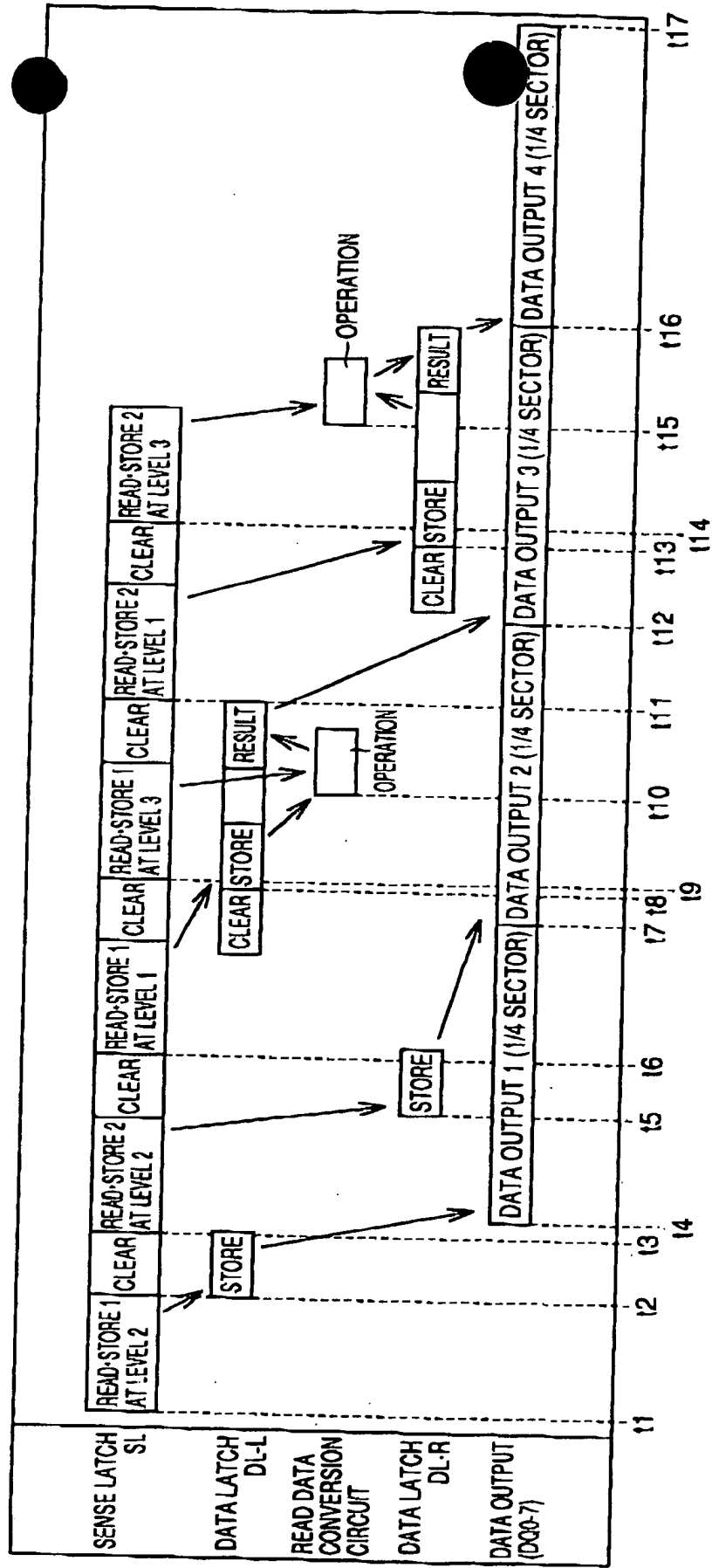


FIG.31

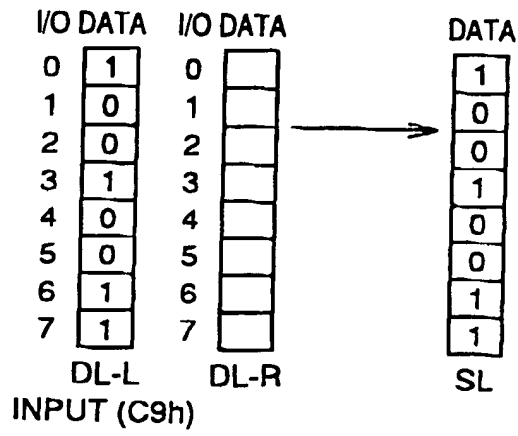


FIG.32

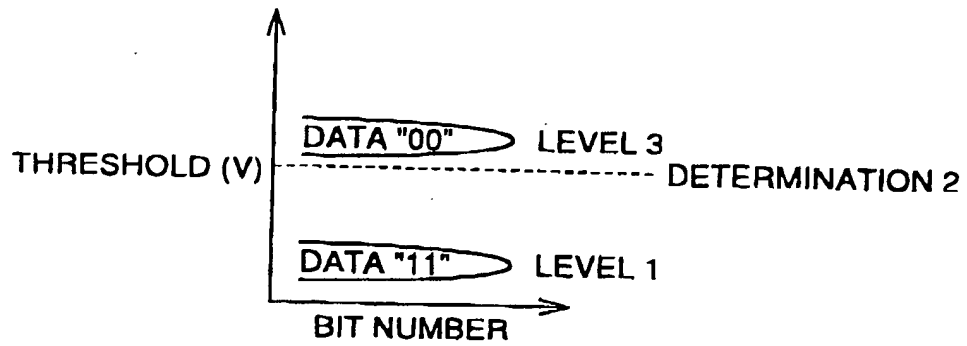


FIG.33

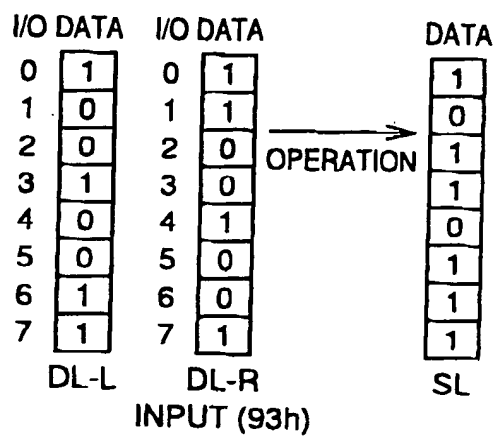


FIG.34

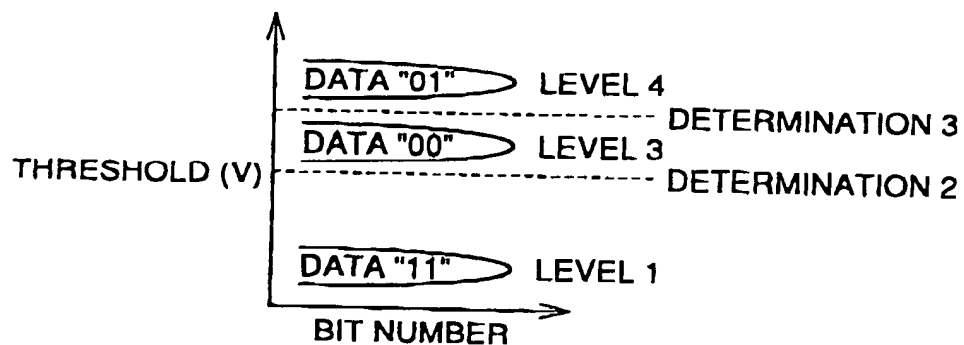


FIG.35

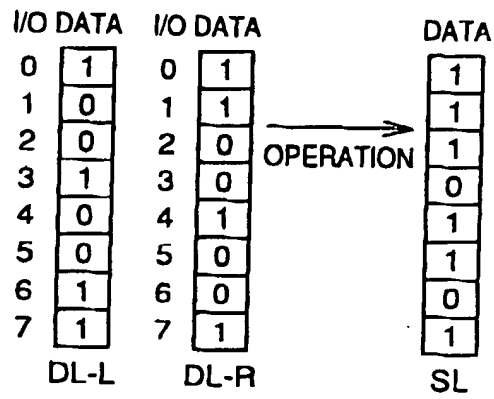


FIG.36

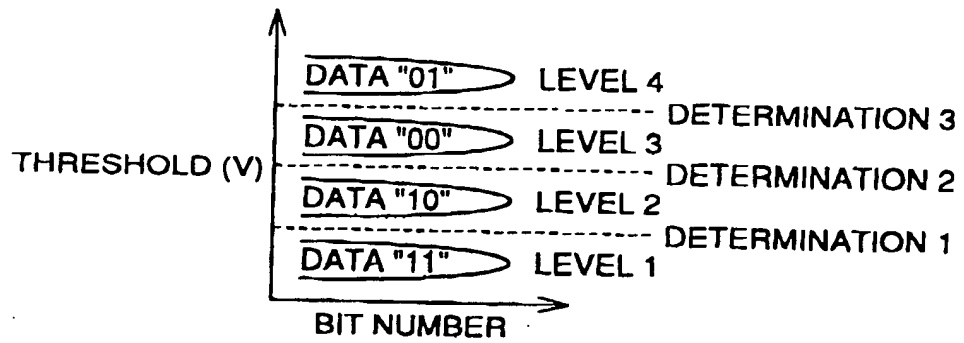


FIG. 37

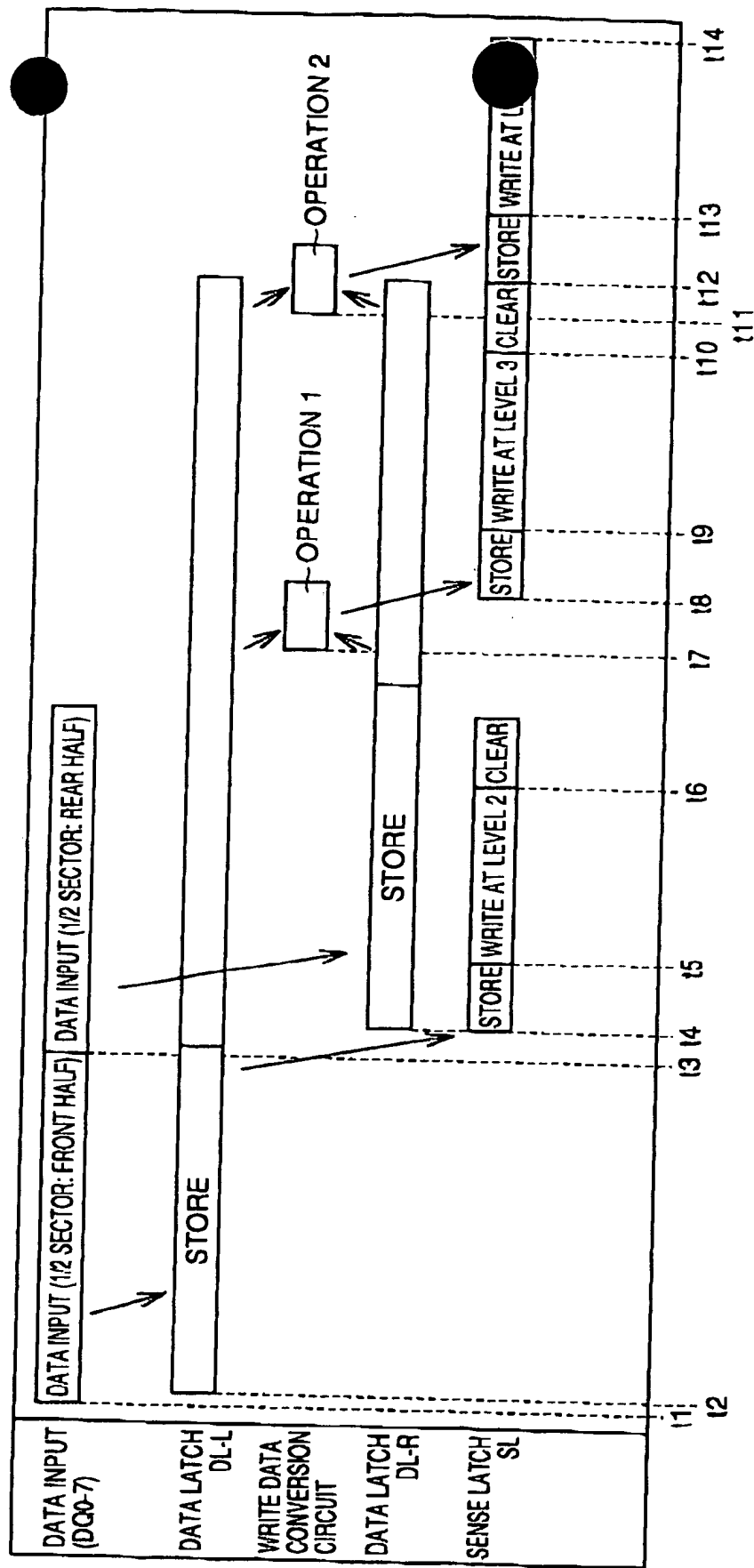


FIG.38

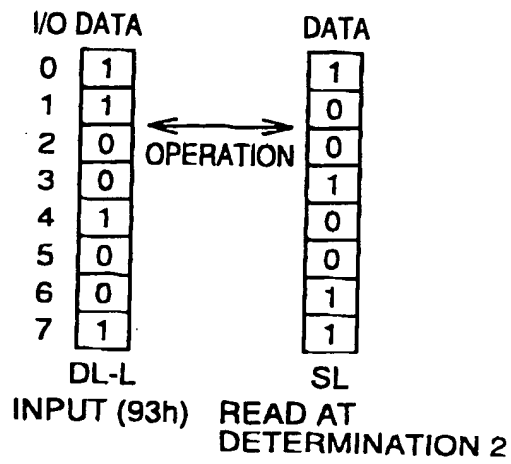


FIG.39

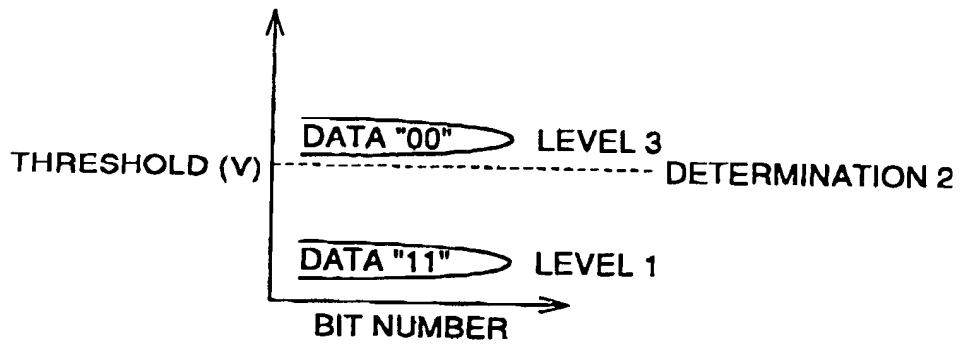


FIG.40

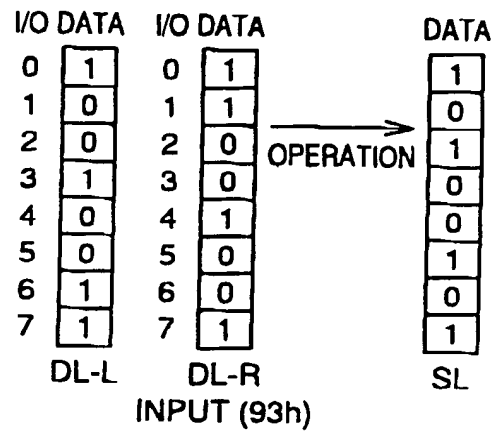


FIG.41

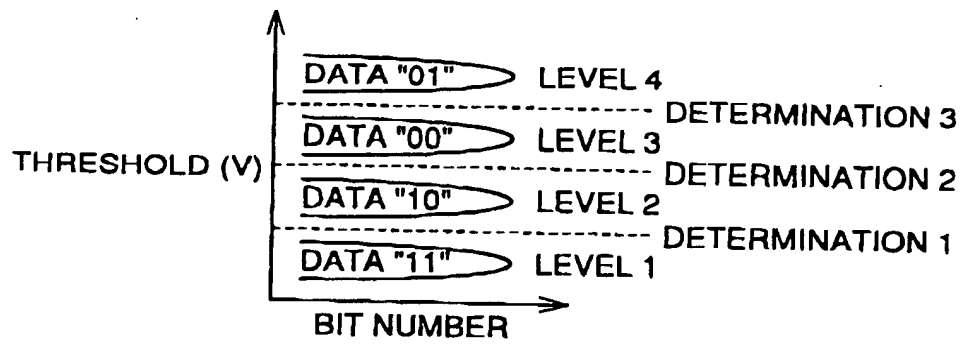
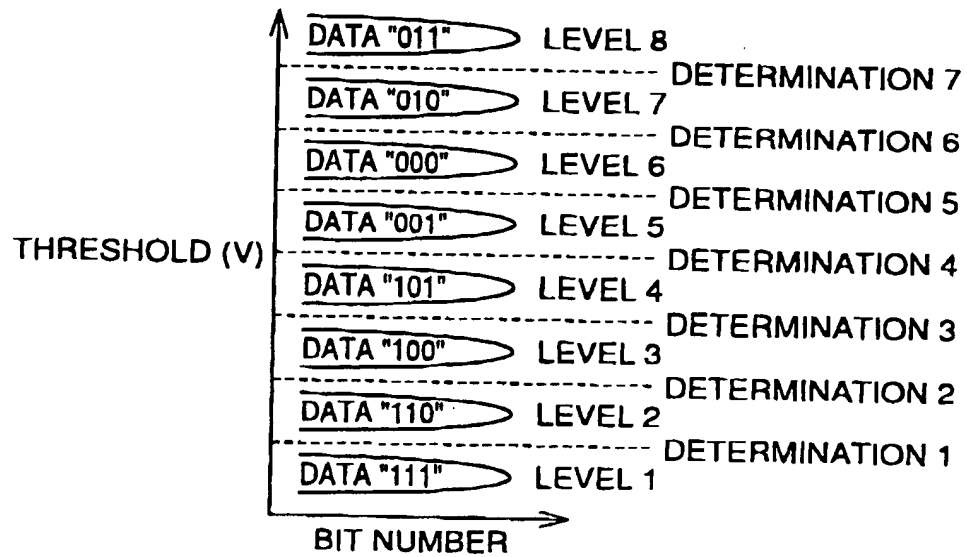


FIG.42

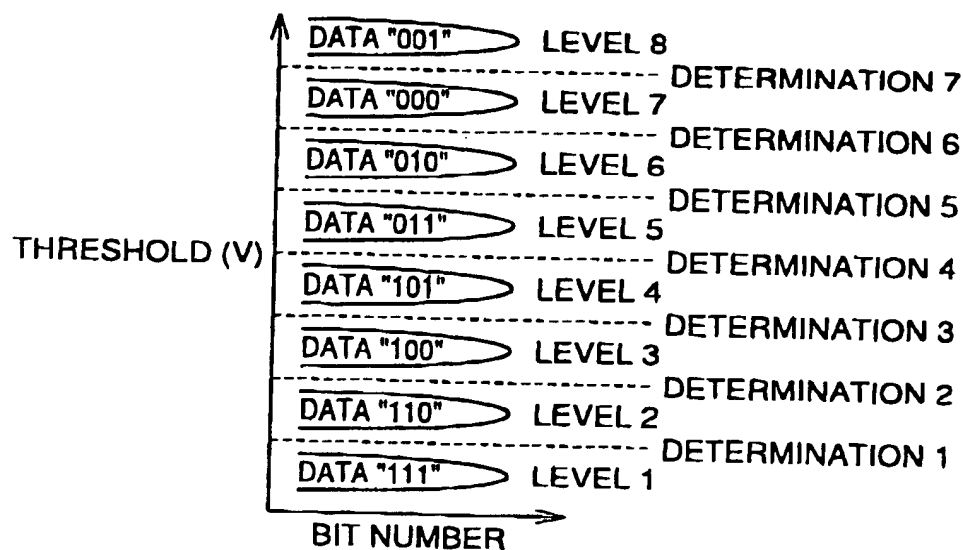


MOST SIGNIFICANT BIT DEFINED  
AT DETERMINATION 4  
INTERMEDIATE BIT DEFINED  
AT DETERMINATION 2 & 6  
LEAST SIGNIFICANT BIT DEFINED  
AT DETERMINATION 1, 3, 5 & 7

OK

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FIG.43



MOST SIGNIFICANT BIT DEFINED  
AT DETERMINATION 4  
"0" & "1" AT LEVELS 3, 4, 5 & 6  
AT DETERMINATION 2 & 6  
NOT DEFINED  
LEAST SIGNIFICANT BIT DEFINED  
AT DETERMINATION 1, 3, 5 & 7

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FIG.44

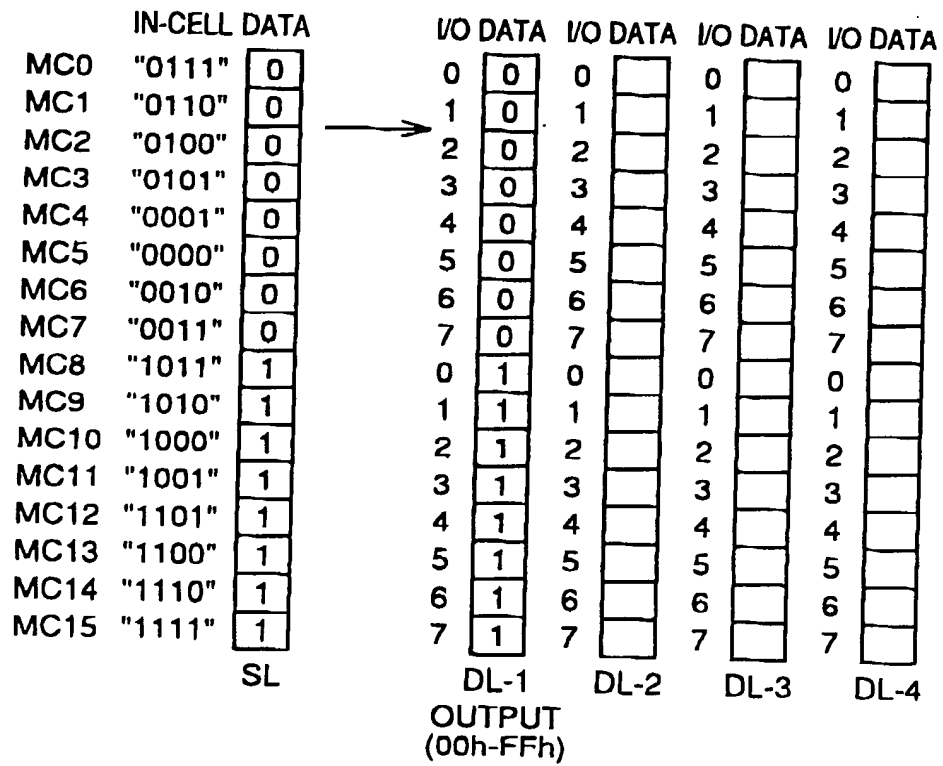


FIG.45

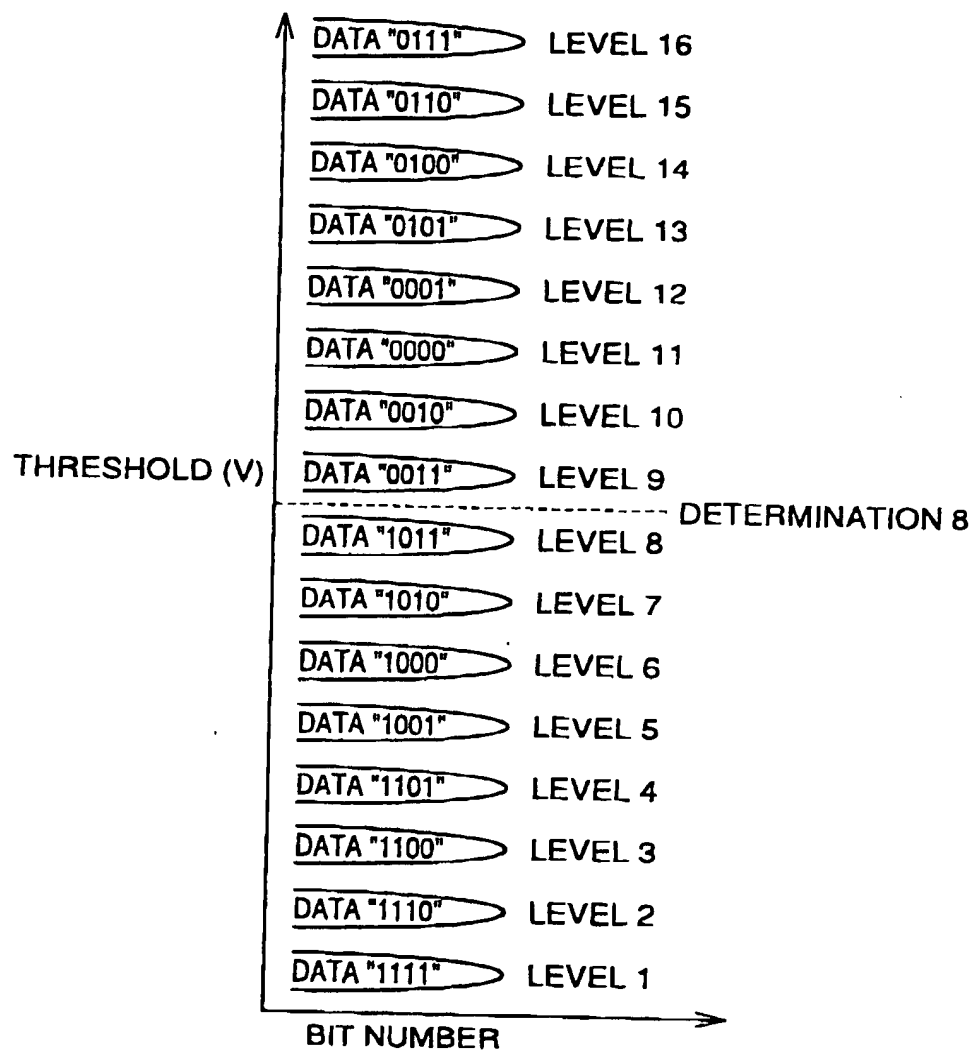


FIG.46

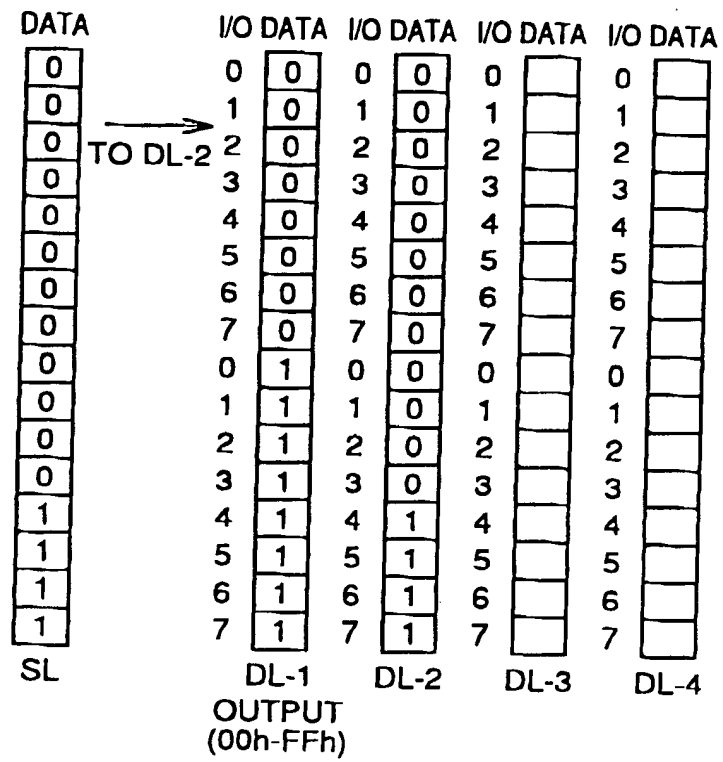
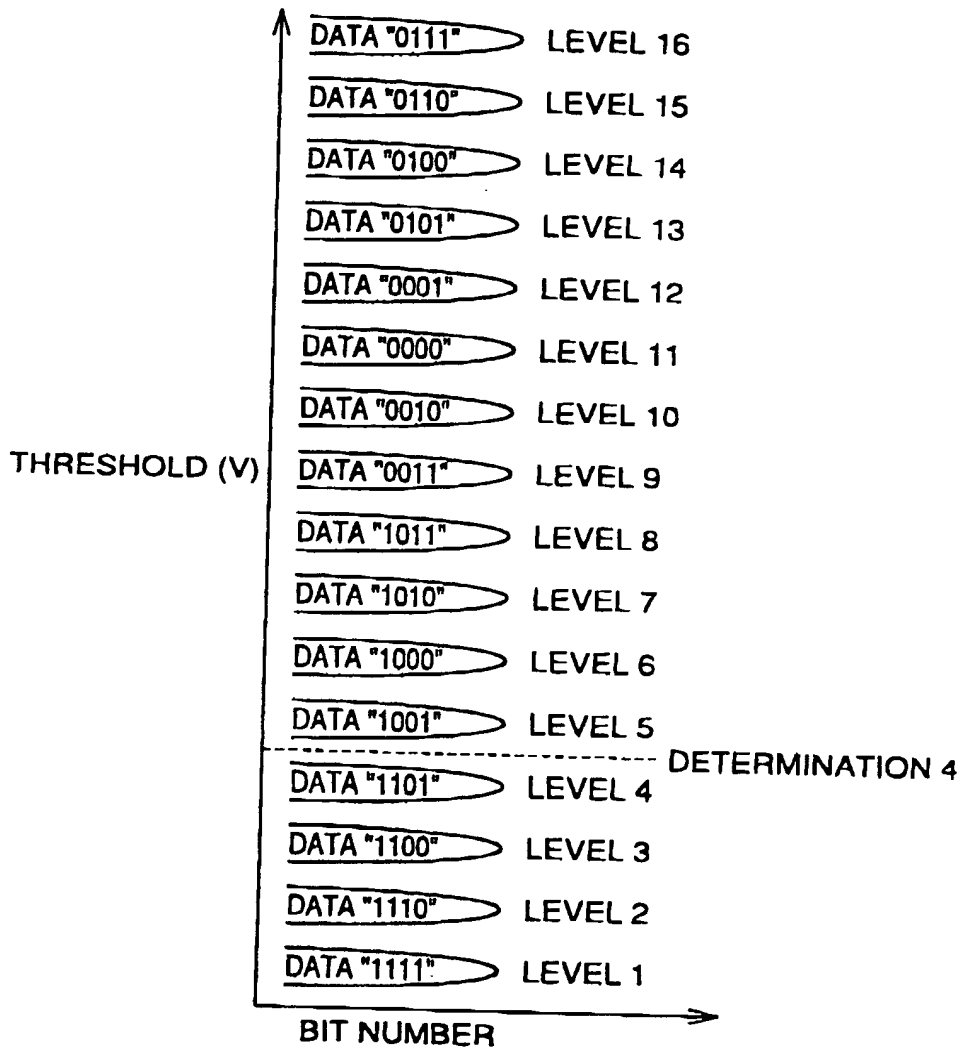


FIG.47



0000000000000000

FIG.48

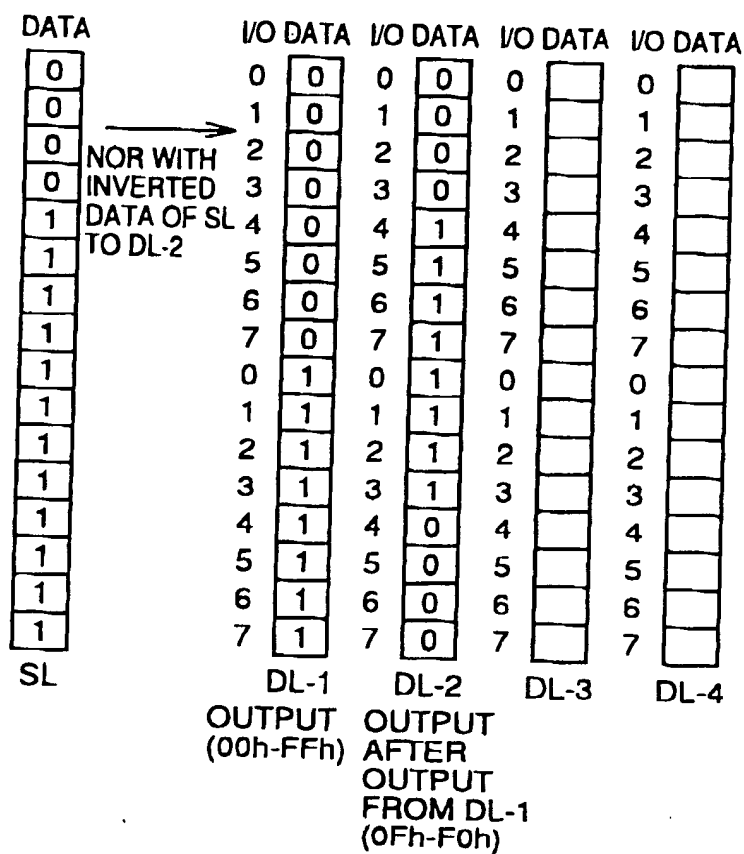
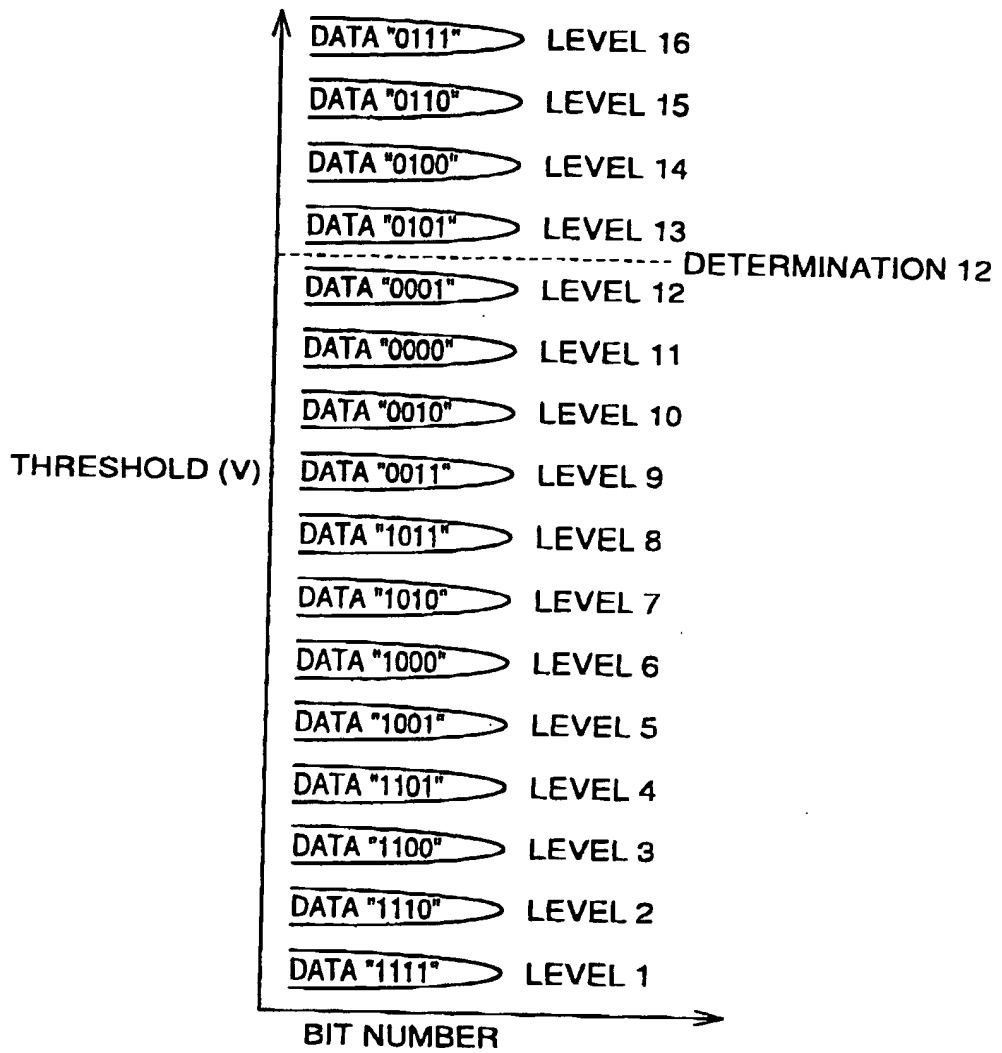


FIG.49



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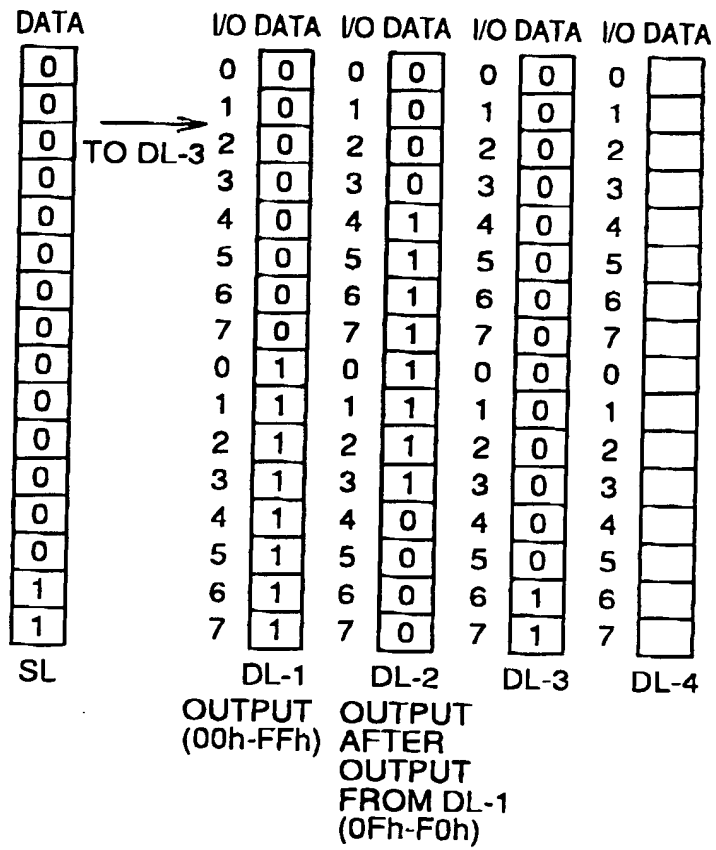
[illegible]

FIG.51

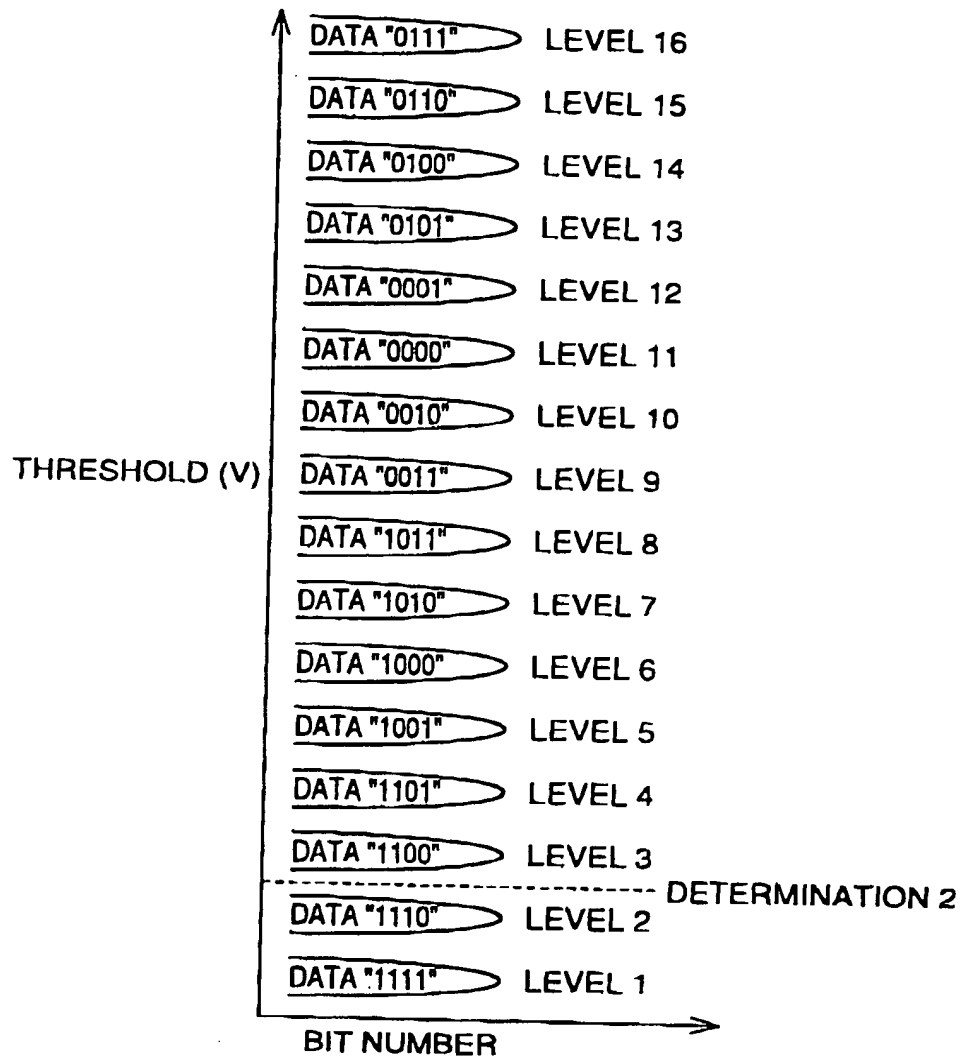


FIG.52

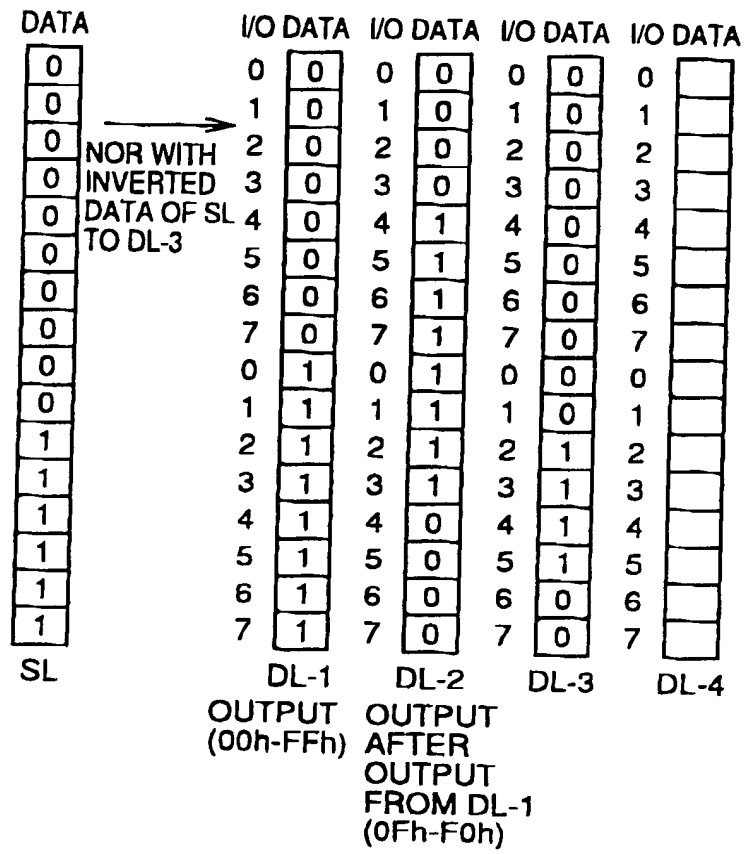


FIG.53

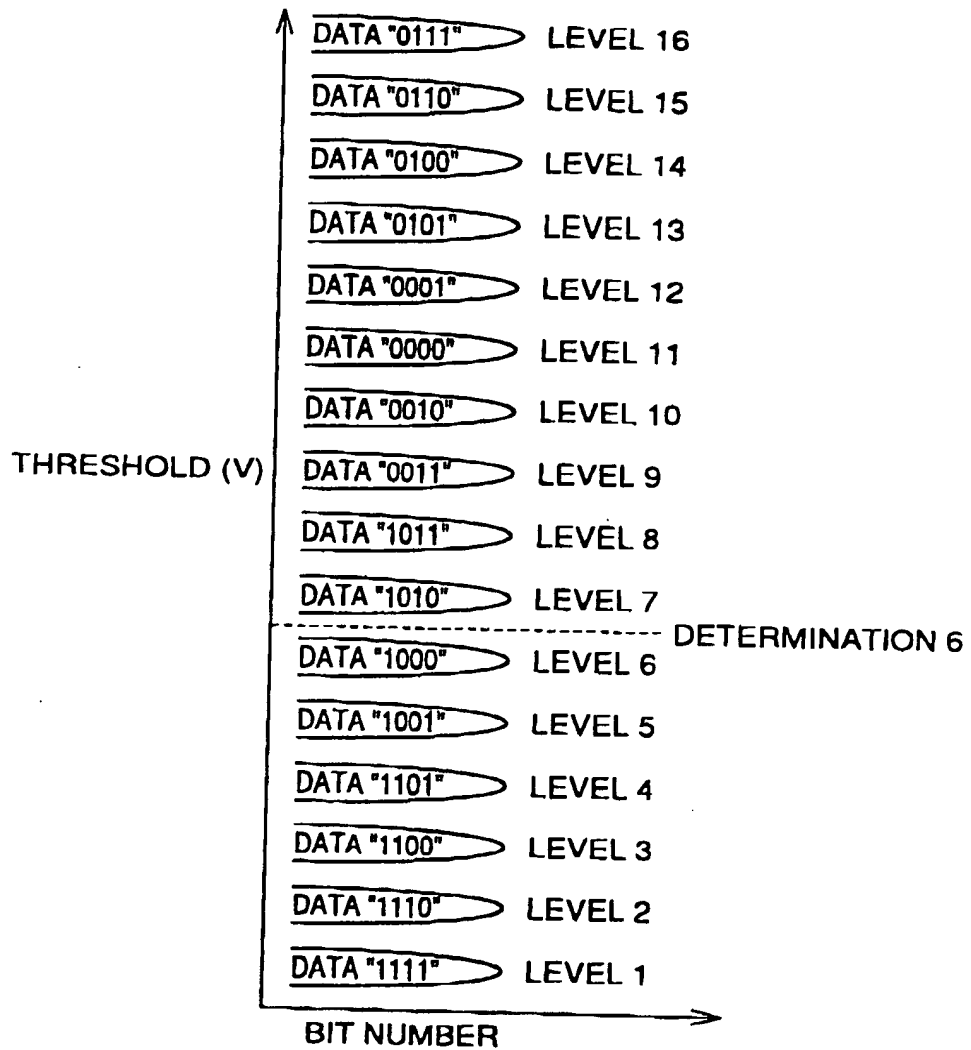


FIG.54

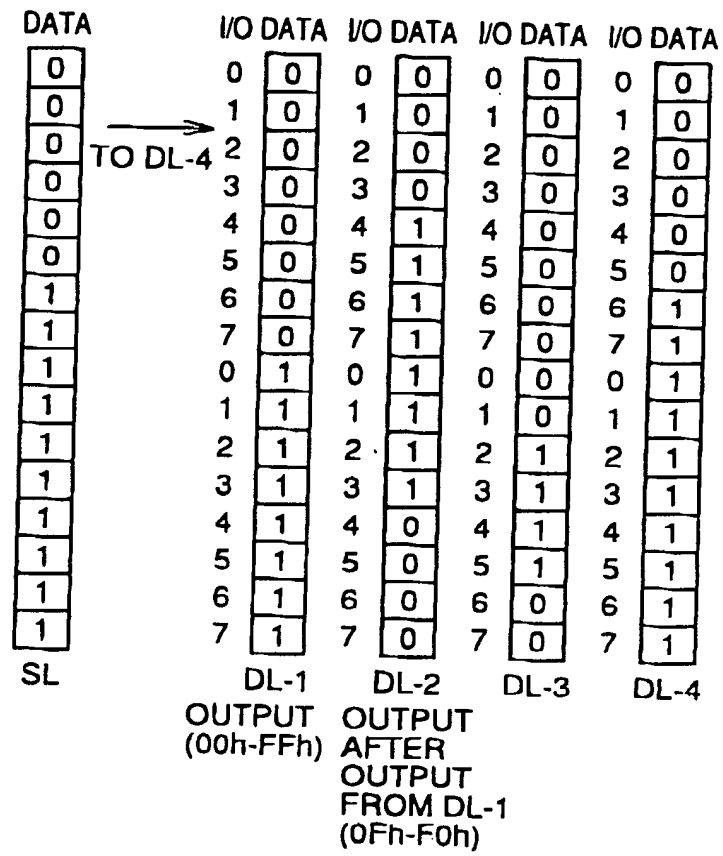
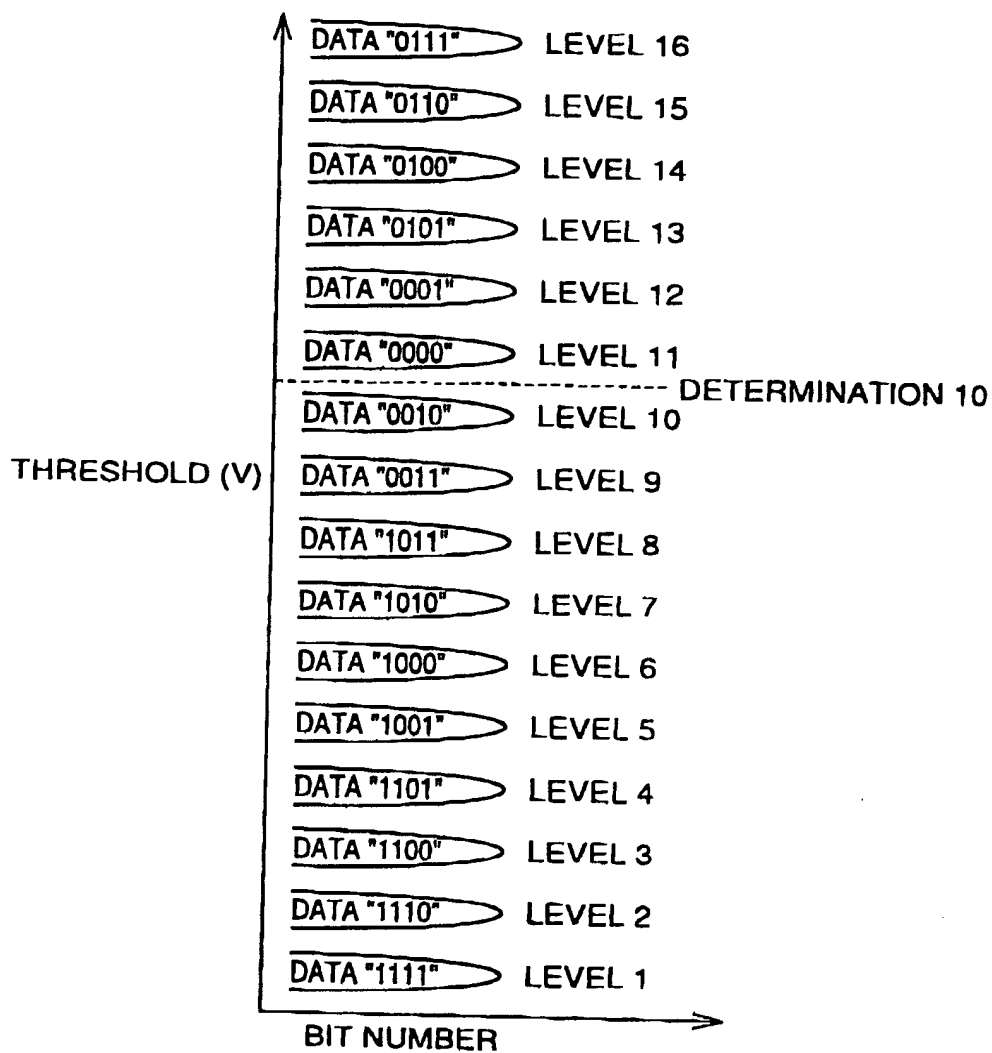


FIG.55

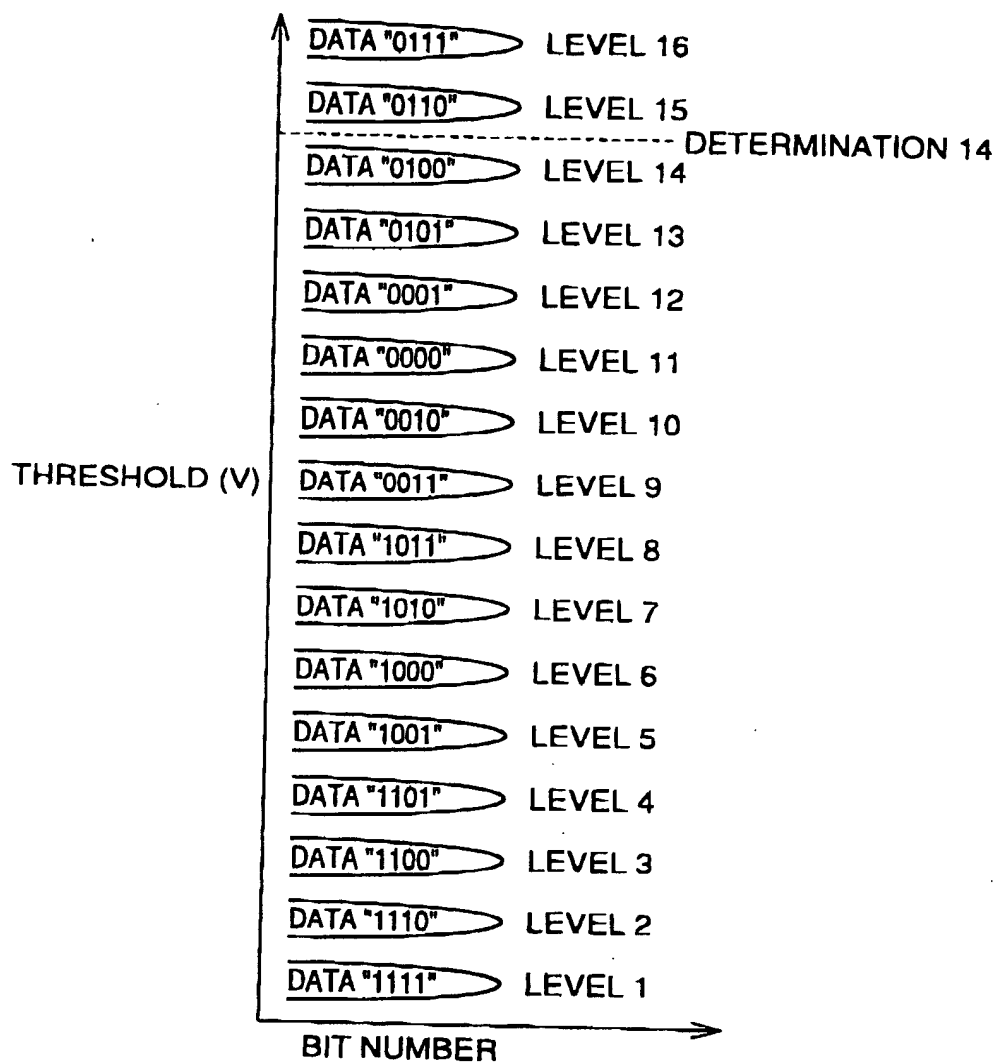


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FIG.56

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0 0	0 0	0 0	0 0
0		1 0	1 0	1 0	1 0
1		2 0	2 0	2 0	2 1
1	NOR	3 0	3 0	3 0	3 1
1	INVERTED	4 0	4 1	4 0	4 1
1	DATA OF SL	5 0	5 1	5 0	5 1
1	AND DATA	6 0	6 1	6 0	6 0
1	OF DL-4	7 0	7 1	7 0	7 0
1	TO DL-4	0 1	0 1	0 0	0 0
1		1 1	1 1	1 0	1 0
1		2 1	2 1	2 1	2 0
1		3 1	3 1	3 1	3 0
1		4 1	4 0	4 1	4 0
1		5 1	5 0	5 1	5 0
1		6 1	6 0	6 0	6 0
1		7 1	7 0	7 0	7 0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT	OUTPUT		
		(00h-FFh)	AFTER		
			OUTPUT		
			FROM DL-1		
			(0Fh-F0h)		

FIG.57



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FIG.58

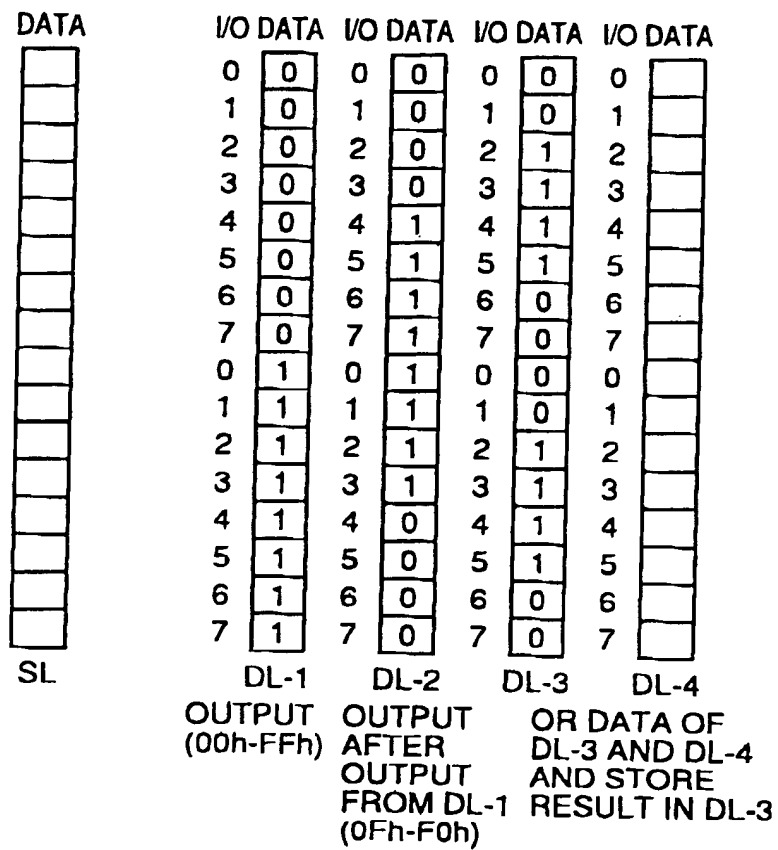


FIG.59

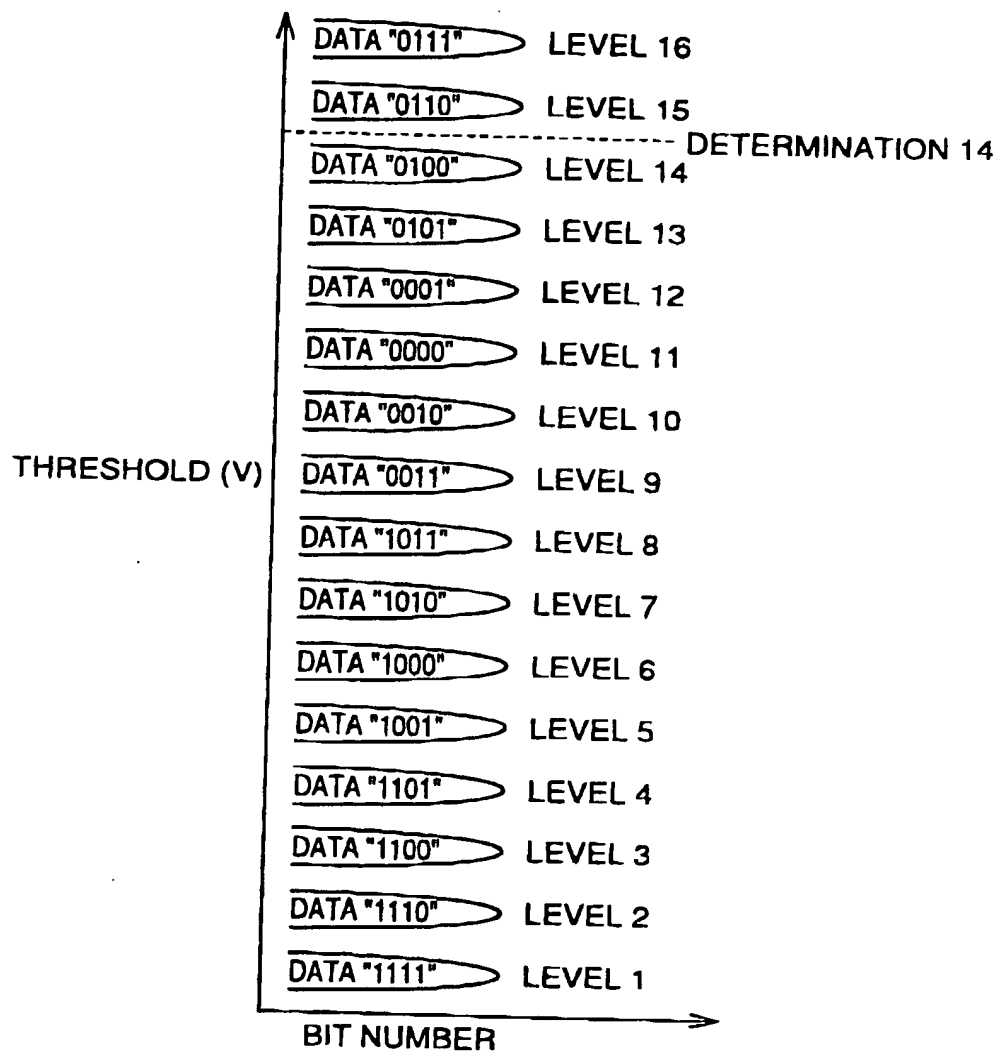


FIG.60

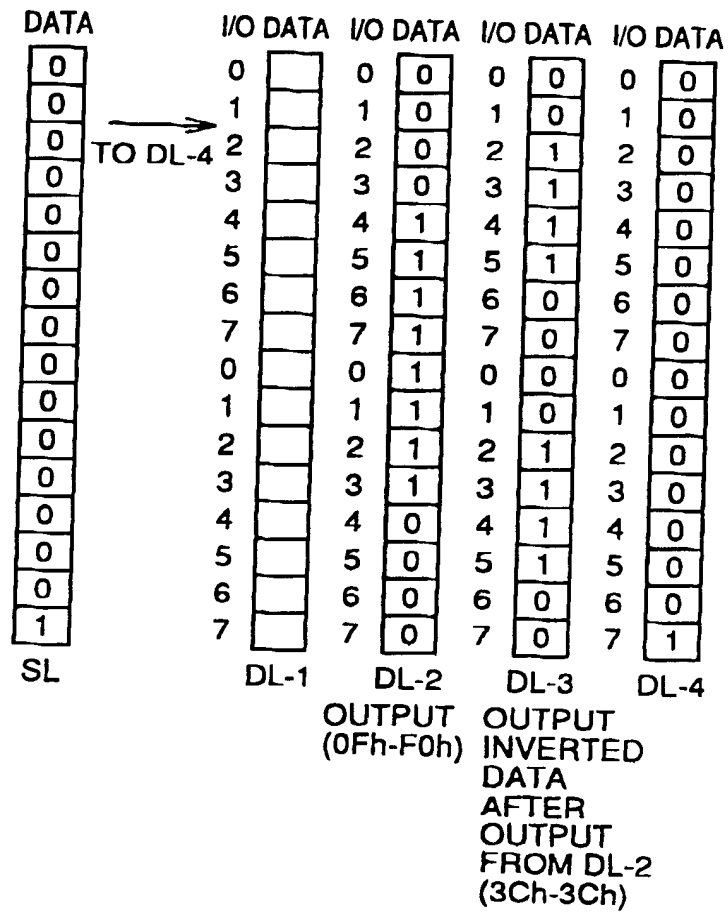
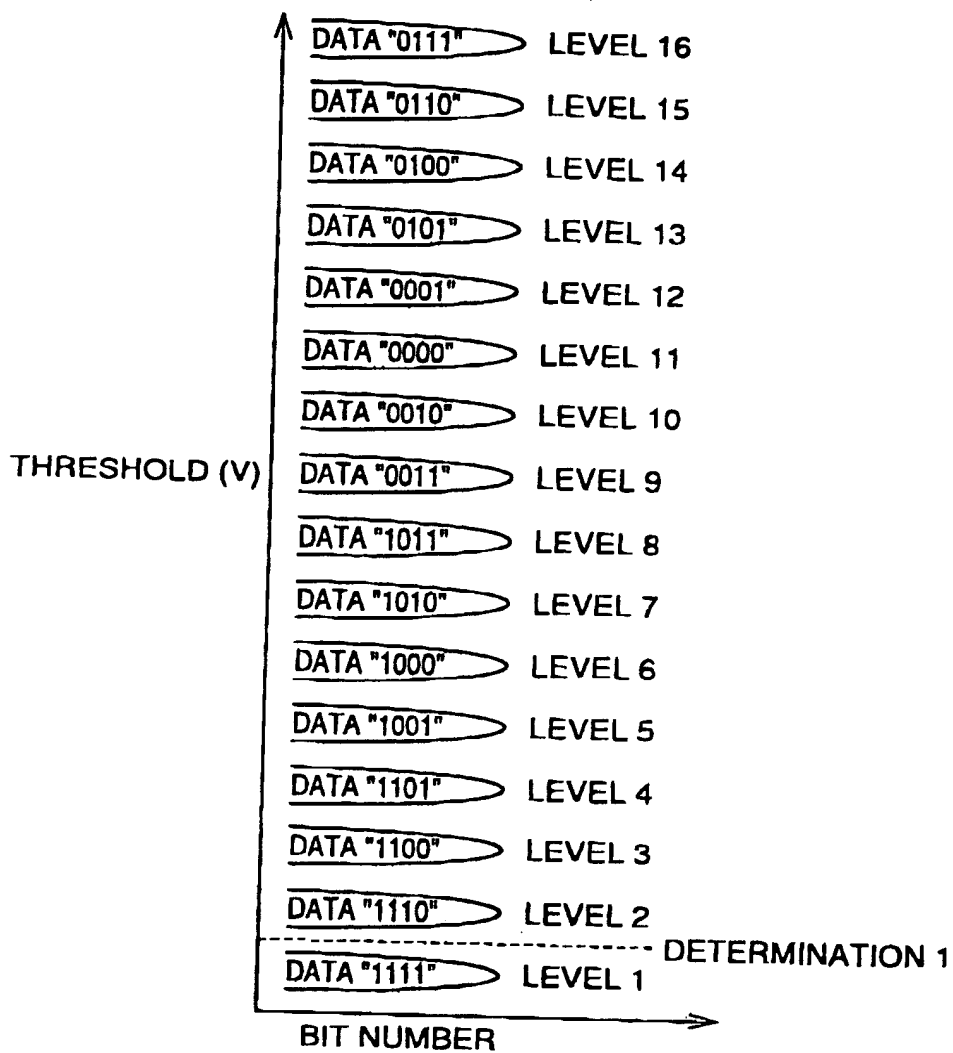


FIG.61



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FIG.62

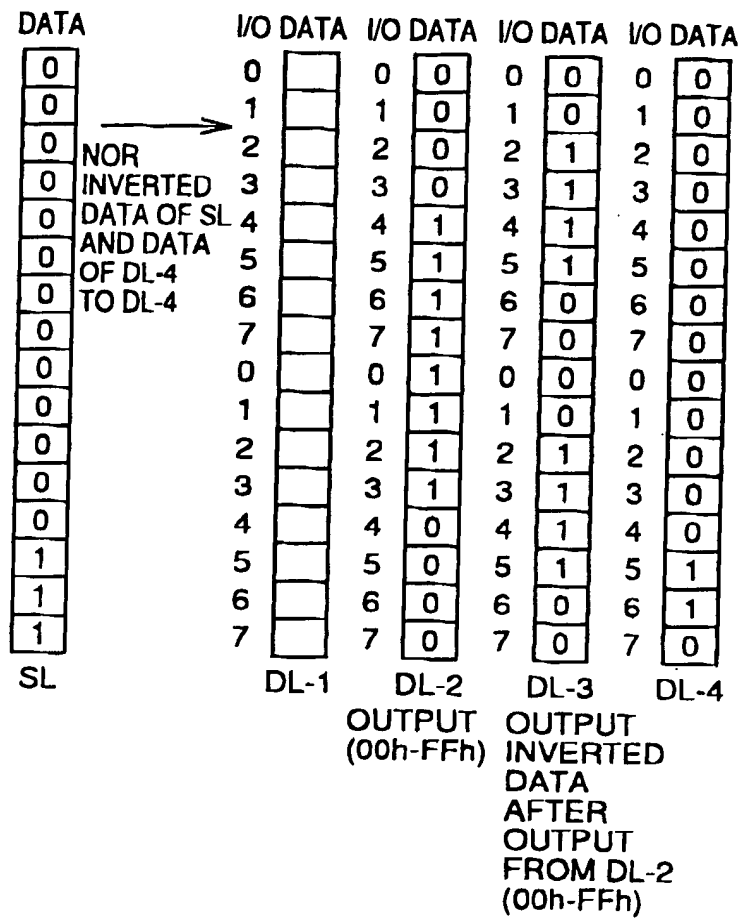
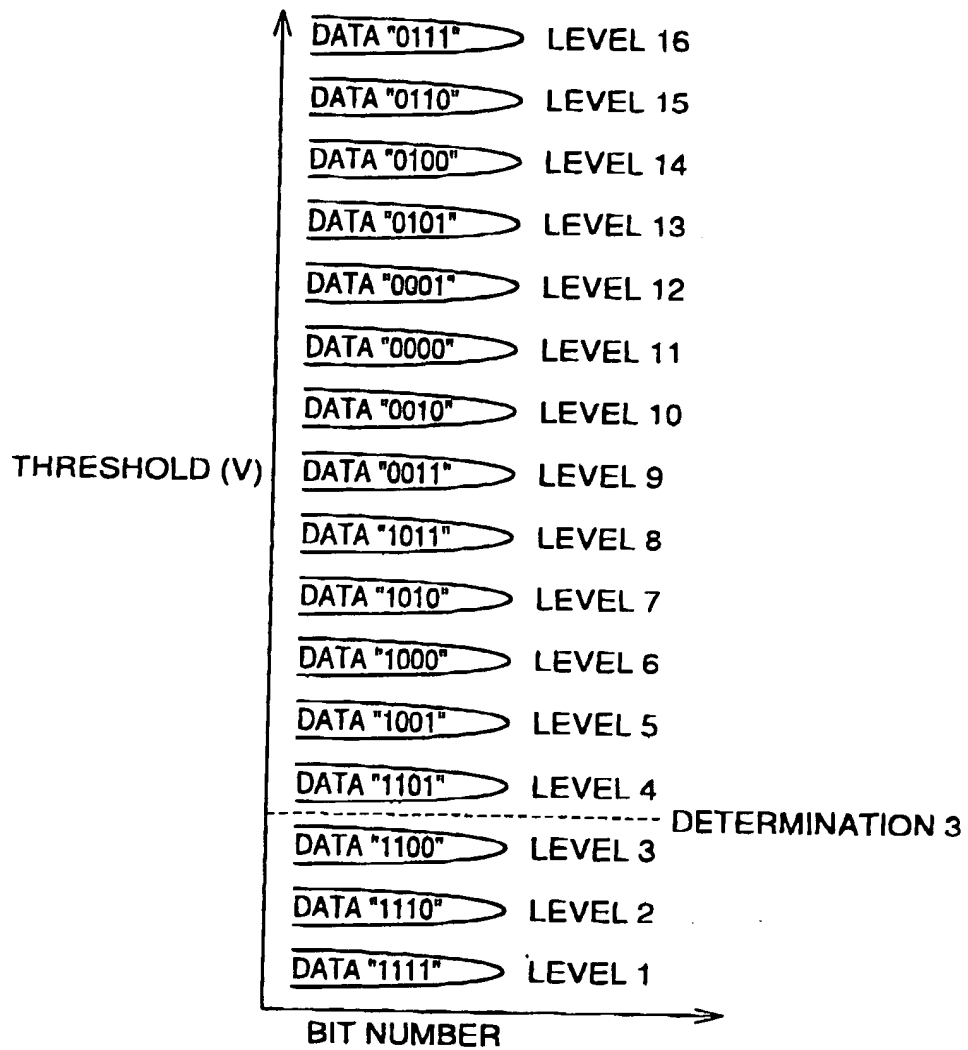


FIG.63



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FIG.64

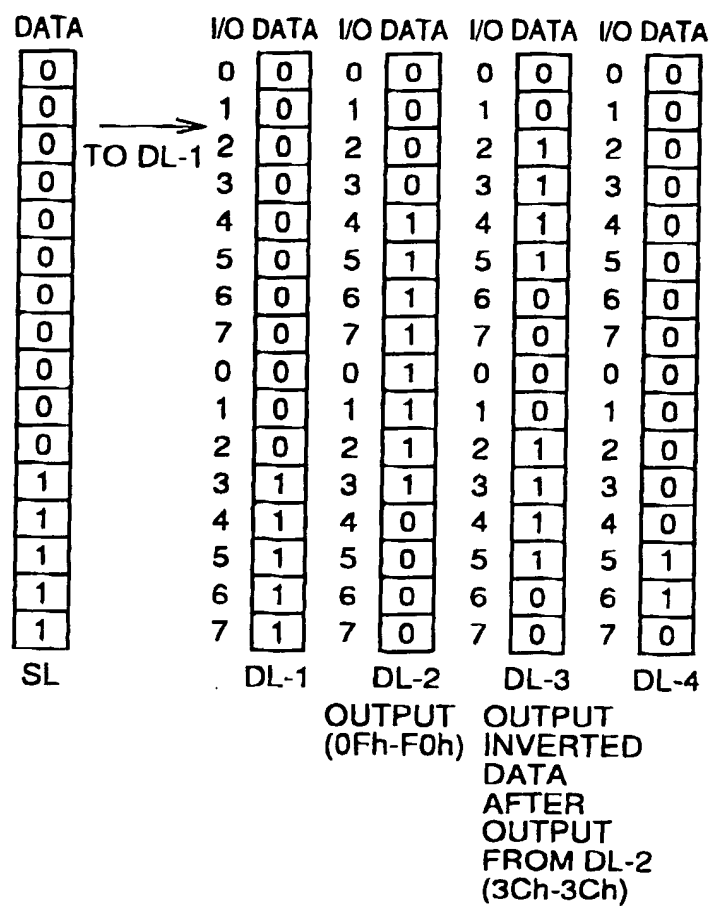
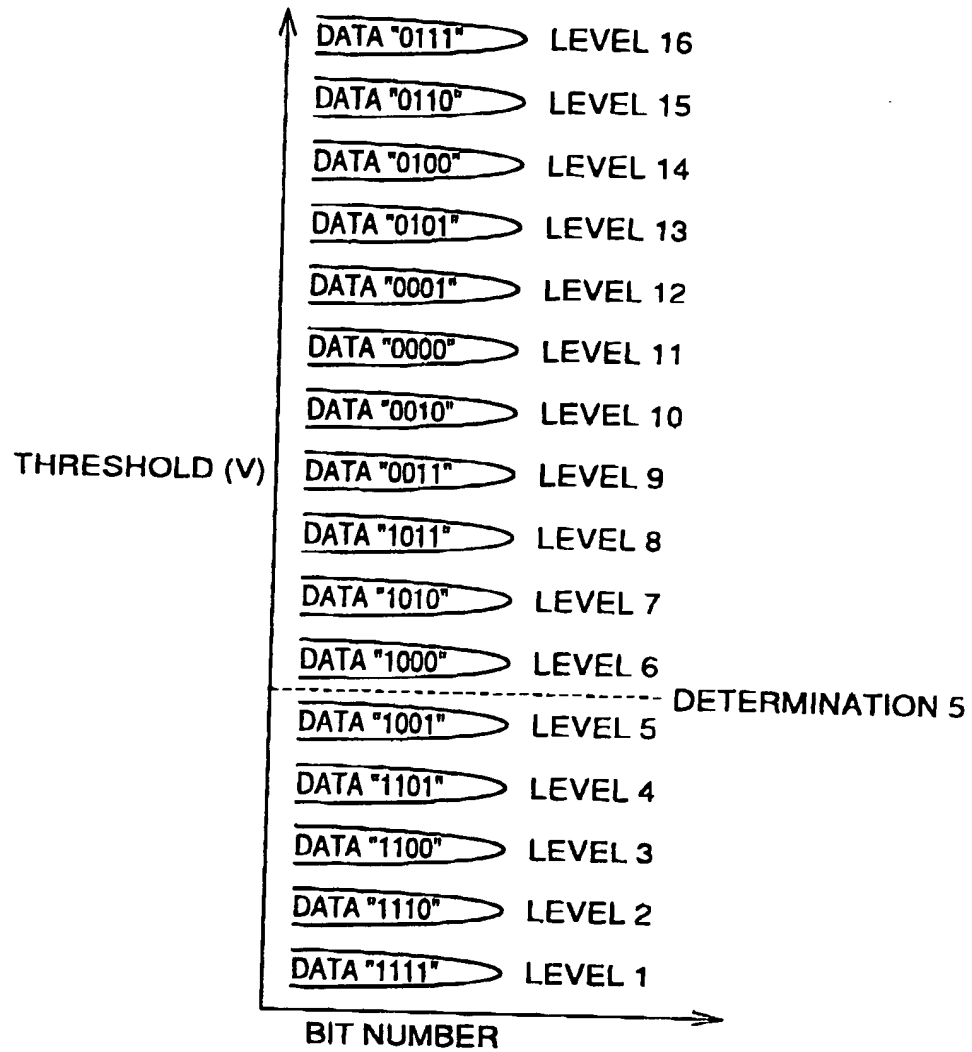


FIG.65



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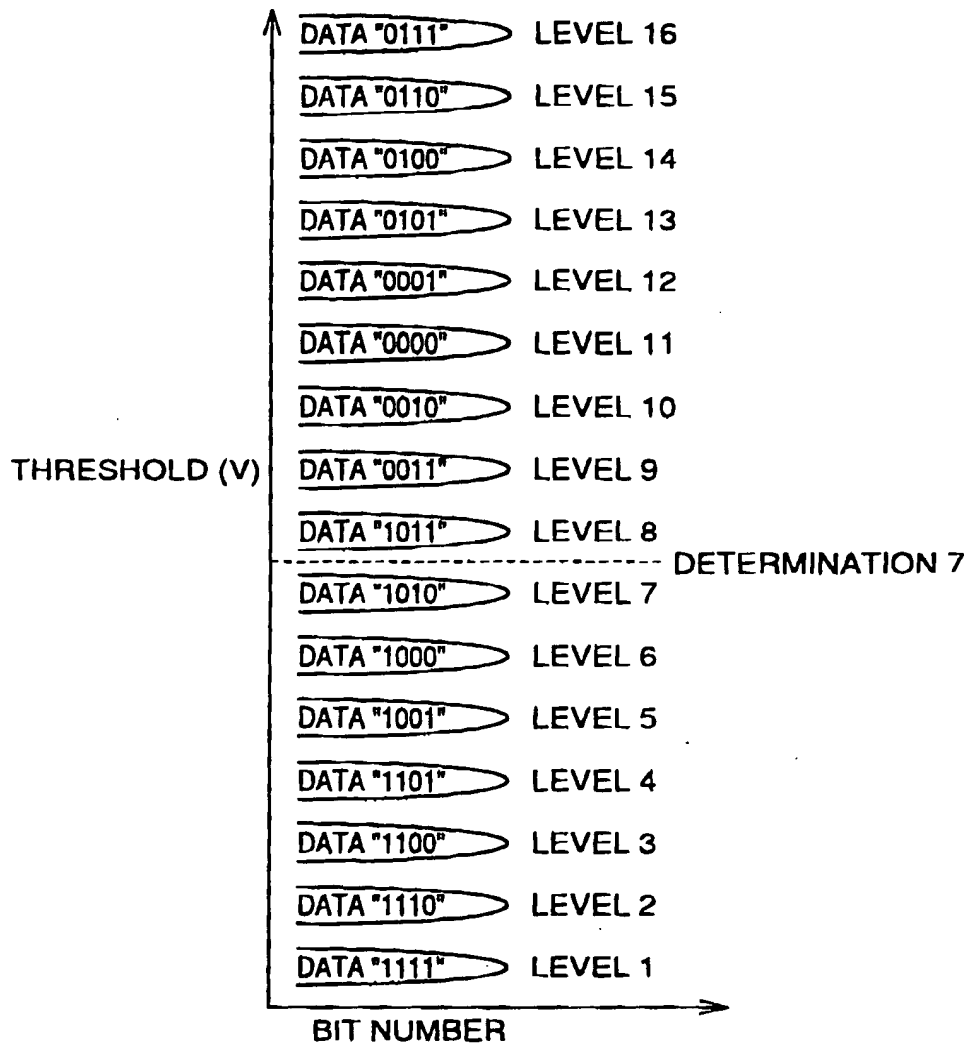
FIG.66

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0		2	0	2	1
0	NOR	3	0	3	1
0	INVERTED	4	0	4	1
0	DATA OF SL	5	0	5	1
0	AND DATA	6	0	6	0
0	OF DL-1	7	0	7	0
0	TO DL-1	0	0	0	0
0		1	1	1	0
1		2	1	2	1
1		3	0	3	1
1		4	0	4	1
1		5	0	5	1
1		6	0	6	0
1		7	0	7	0
SL		DL-1	DL-2	DL-3	DL-4

OUTPUT (00h-FFh)      OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (00h-FFh)

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FIG.67



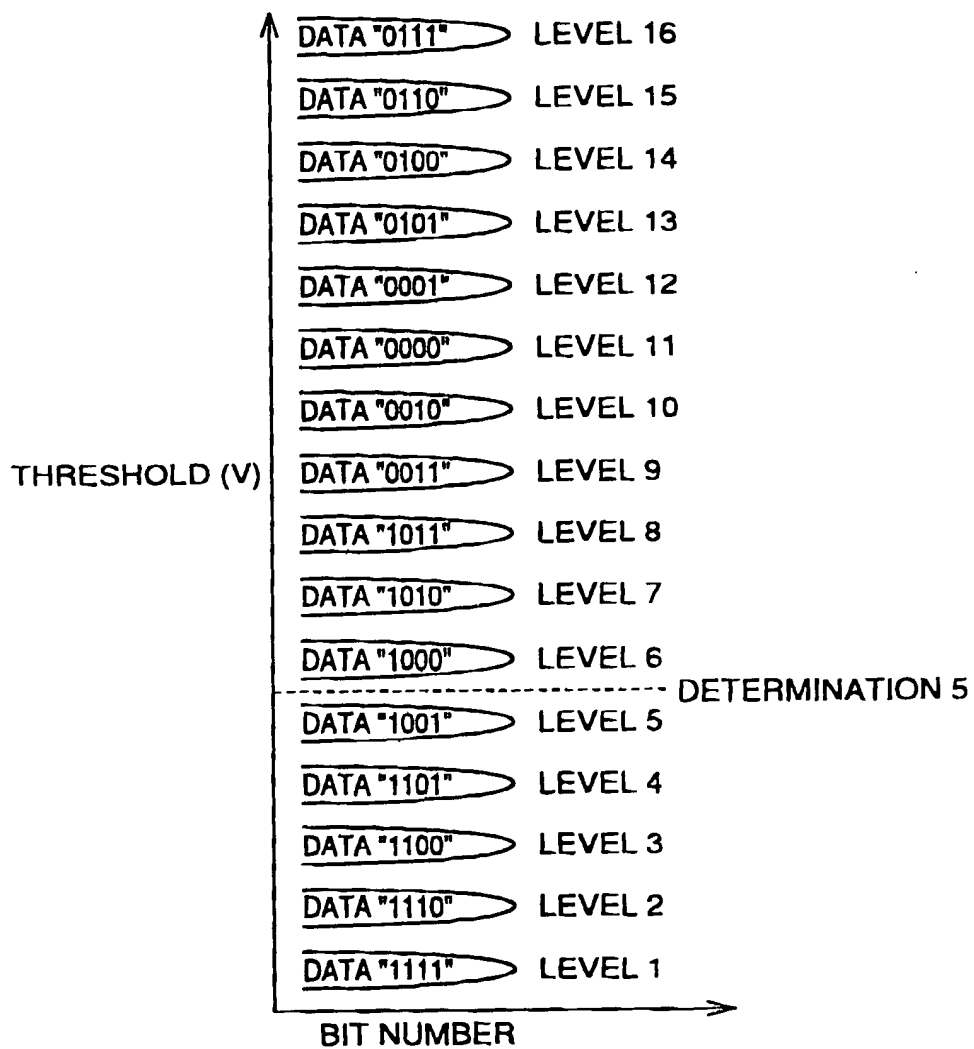
65222T 46469460

FIG.68

		OR DATA OF DL-1 AND DL-4 TO DL-4							
DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
		0	0	0	0	0	0	0	0
		1	0	1	0	1	0	1	0
		2	0	2	0	2	1	2	0
		3	0	3	0	3	1	3	0
		4	0	4	1	4	1	4	0
		5	0	5	1	5	1	5	0
		6	0	6	1	6	0	6	0
		7	0	7	1	7	0	7	0
		0	0	0	1	0	0	0	0
		1	1	1	1	1	0	1	1
		2	1	2	1	2	1	2	1
		3	0	3	1	3	1	3	0
		4	0	4	0	4	1	4	0
		5	0	5	0	5	1	5	1
		6	0	6	0	6	0	6	1
		7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	
		OUTPUT (0Fh-F0h)				OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)			

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FIG.69



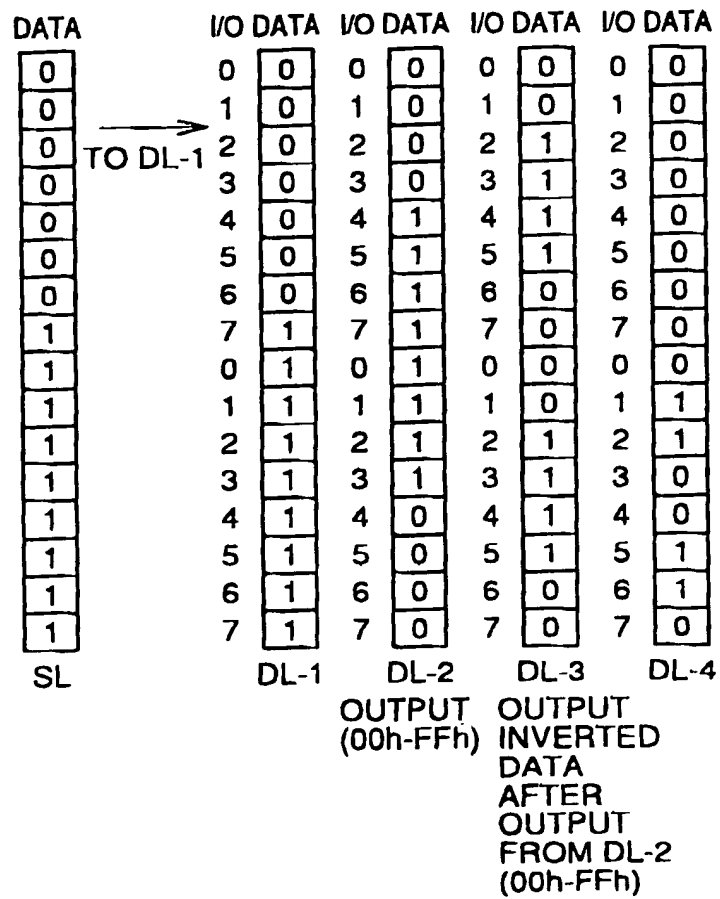
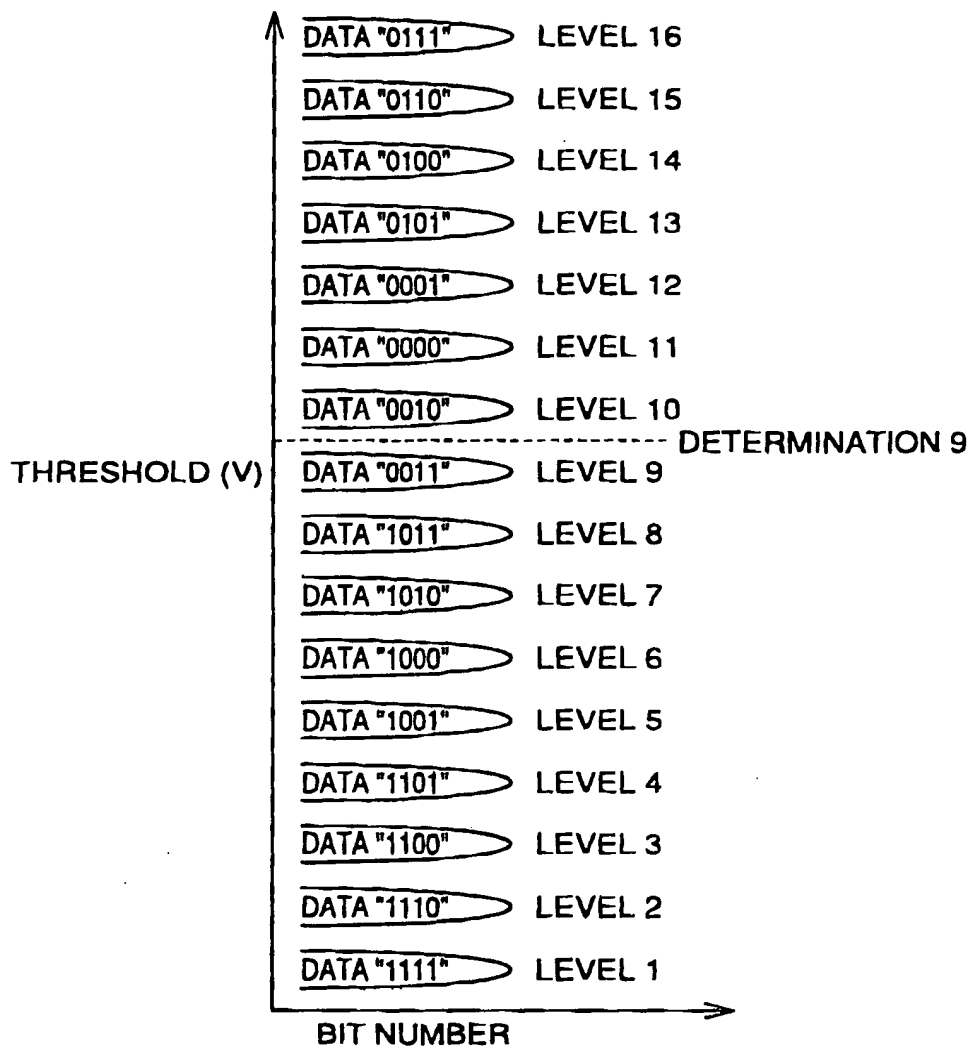
[illegible]

FIG. 71



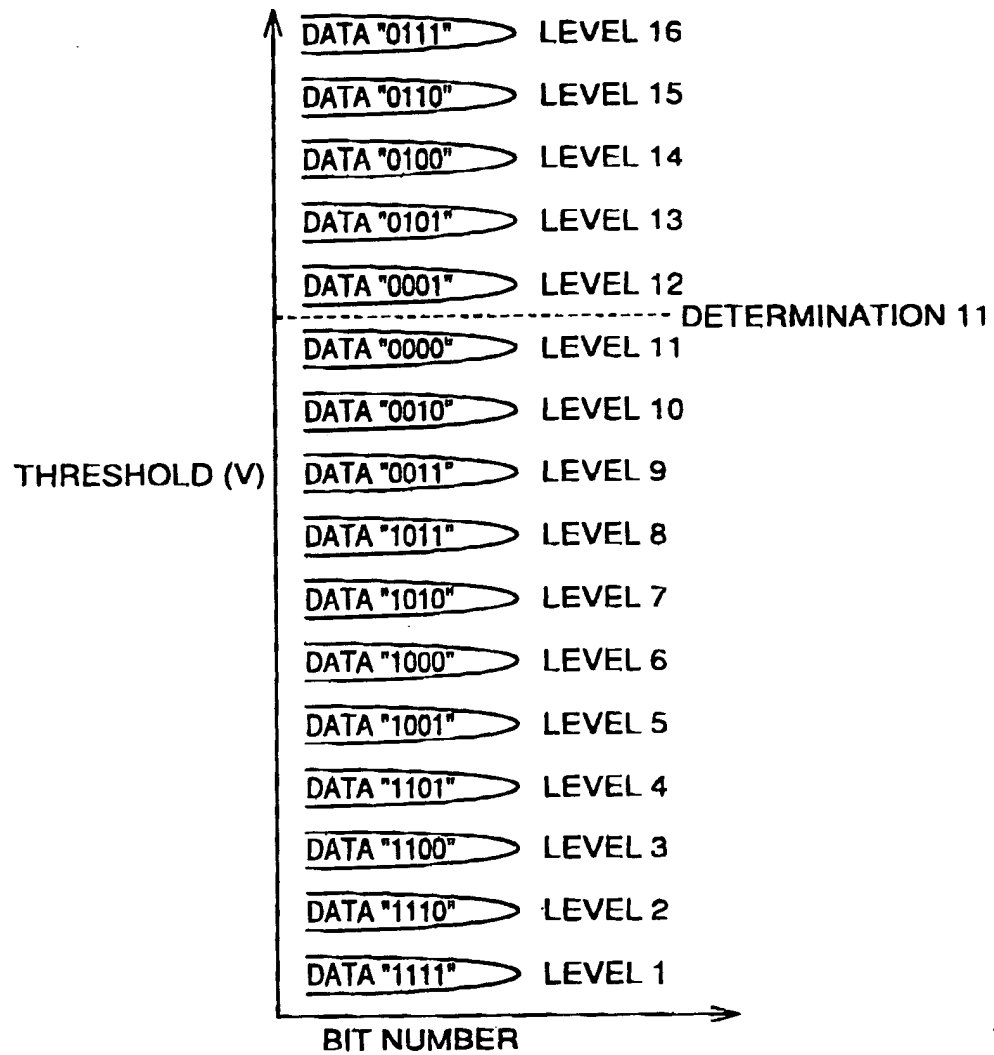
55222T" 25469460

FIG.72

DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA
0		0	0	0	0
0		1	0	1	0
0		2	0	2	1
0	NOR	3	0	3	1
0	INVERTED	4	0	4	1
1	DATA OF SL	5	1	5	1
1	AND DATA	6	1	6	0
1	OF DL-1	7	0	7	0
1	TO DL-1	0	0	0	0
1		1	0	1	0
1		2	0	2	1
1		3	0	3	1
1		4	0	4	1
1		5	0	5	1
1		6	0	6	0
1		7	0	7	0
SL		DL-1	DL-2	DL-3	DL-4
		OUTPUT	OUTPUT		
		(00h-FFh)	INVERTED		
			DATA		
			AFTER		
			OUTPUT		
			FROM DL-2		
			(00h-FFh)		

00000000 00000000 00000000 00000000

FIG.73



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FIG.74

OR DATA OF DL-1 AND DL-4 TO DL-4							
DATA		I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA	I/O DATA
		0	0	0	0	0	0
		1	0	1	0	1	0
		2	0	2	0	2	0
		3	0	3	0	3	0
		4	0	4	1	4	0
		5	1	5	1	5	1
		6	1	6	1	6	0
		7	0	7	1	7	0
		0	0	0	1	0	0
		1	0	1	1	1	0
		2	0	2	1	2	1
		3	0	3	1	3	0
		4	0	4	0	4	1
		5	0	5	0	5	1
		6	0	6	0	6	0
		7	0	7	0	7	0
SL		DL-1	DL-2	DL-3	DL-4		
		OUTPUT (0Fh-F0h)		OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)			

FIG. 75

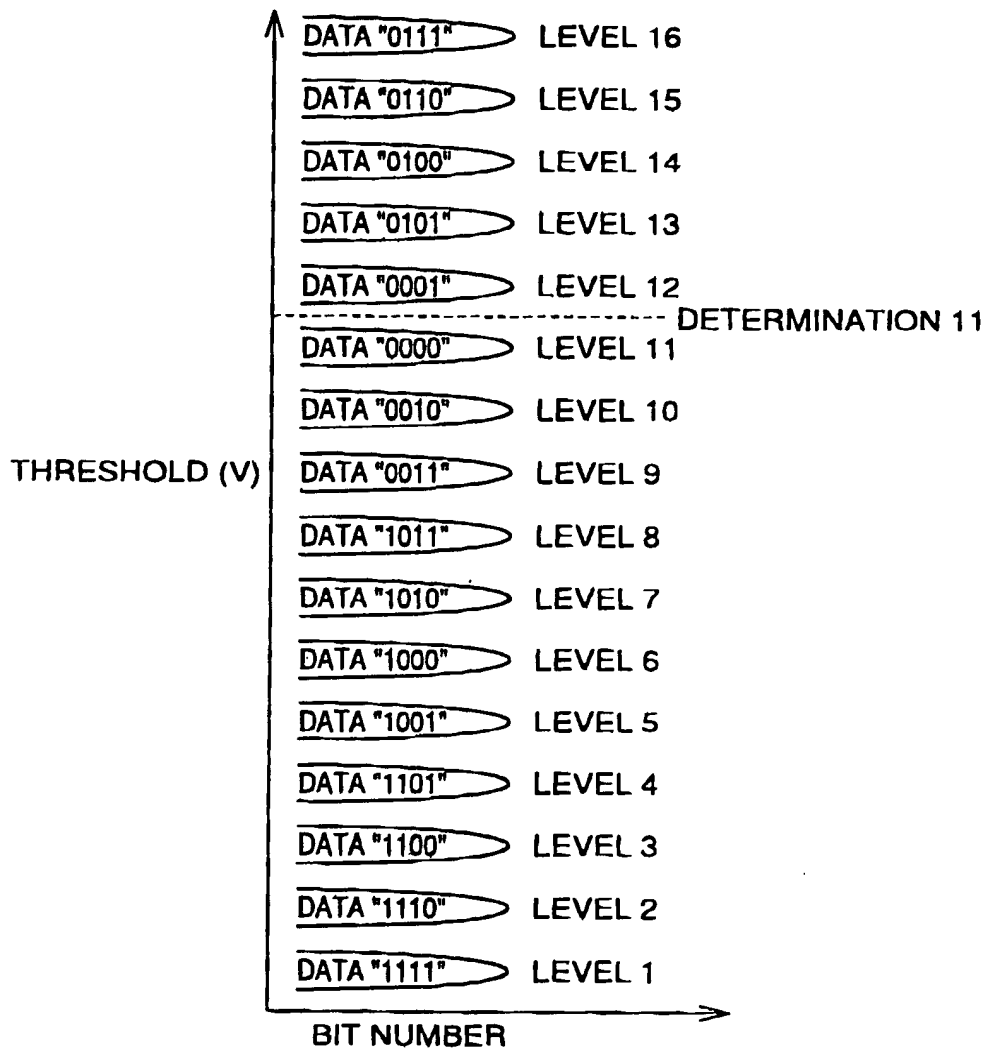


FIG.76

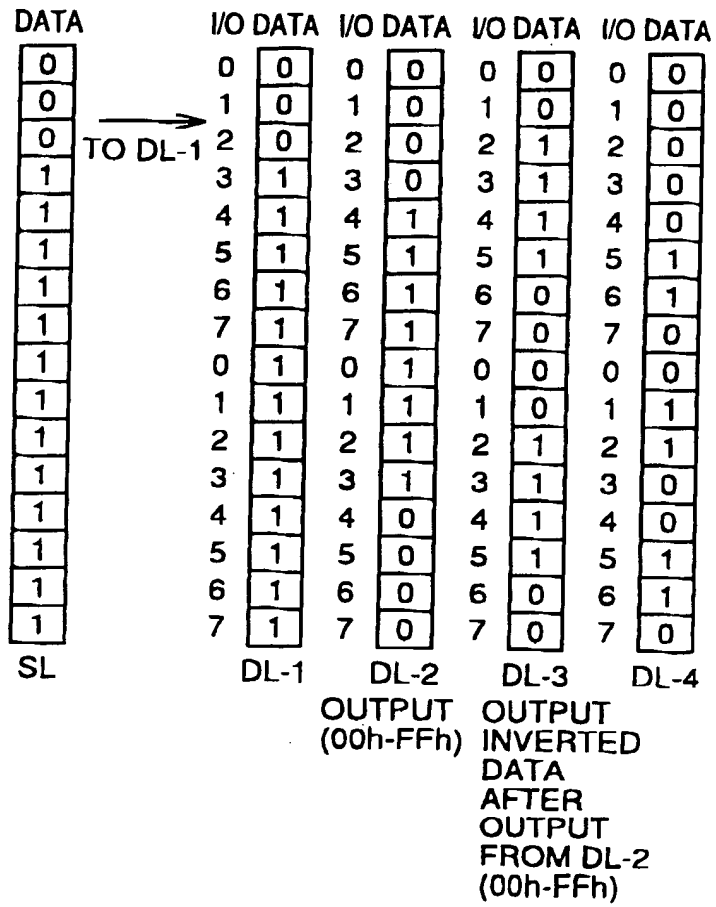
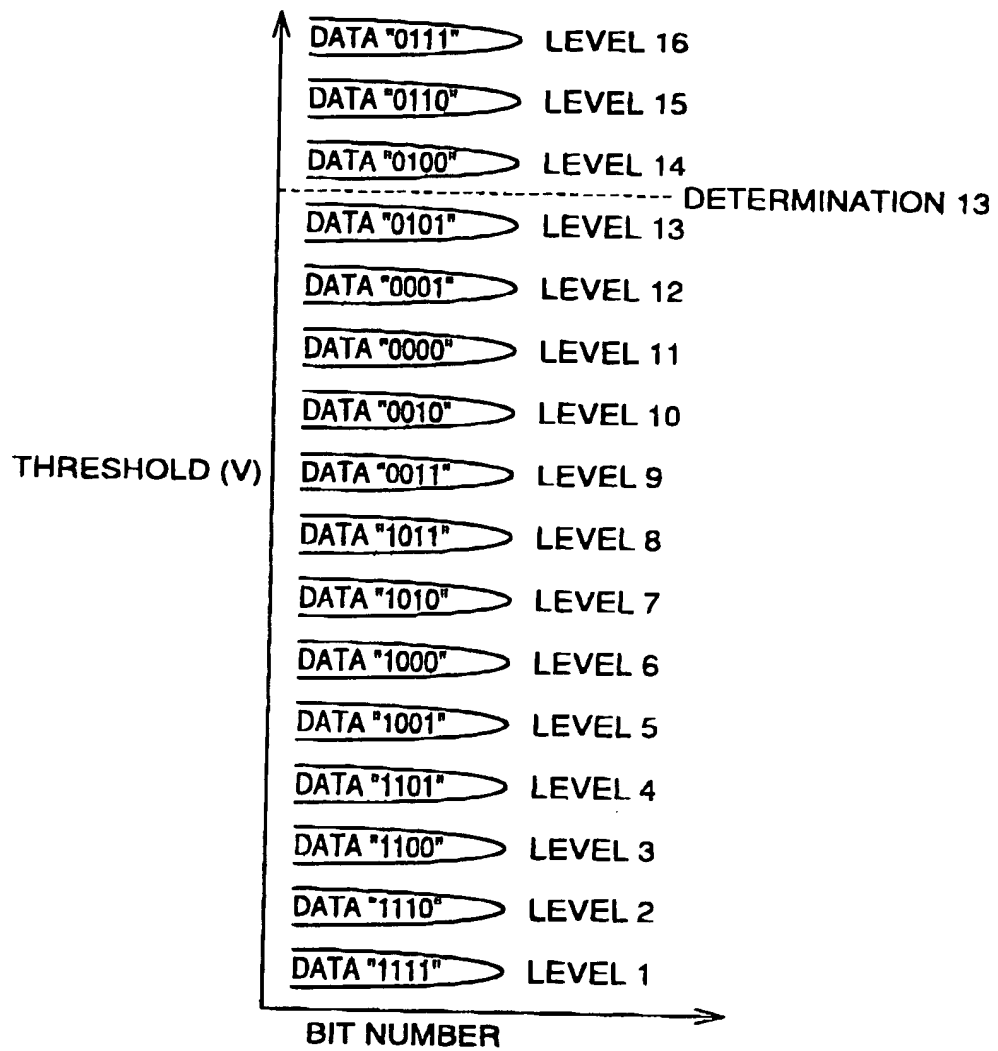


FIG.77



65 23 12 11 10 9 8 7 6 5 4 3 2 1 0

FIG.78

		OR DATA OF DL-1 AND DL-4 TO DL-4							
DATA		I/O DATA		I/O DATA		I/O DATA		I/O DATA	
0	NOR INVERTED DATA OF SL AND DATA OF DL-1 TO DL-1	0	0	0	0	0	0	0	0
1		1	1	1	0	1	0	1	0
1		2	1	2	0	2	1	2	0
1		3	0	3	0	3	1	3	0
1		4	0	4	1	4	1	4	0
1		5	0	5	1	5	1	5	1
1		6	0	6	1	6	0	6	1
1		7	0	7	1	7	0	7	0
1		0	0	0	1	0	0	0	0
1		1	0	1	1	1	0	1	1
1		2	0	2	1	2	1	2	1
1		3	0	3	1	3	1	3	0
1		4	0	4	0	4	1	4	0
1		5	0	5	0	5	1	5	1
1		6	0	6	0	6	0	6	1
1		7	0	7	0	7	0	7	0
SL		DL-1		DL-2		DL-3		DL-4	
		OUTPUT (0Fh-F0h)				OUTPUT INVERTED DATA AFTER OUTPUT FROM DL-2 (3Ch-3Ch)			

6622331 26463450

FIG.79

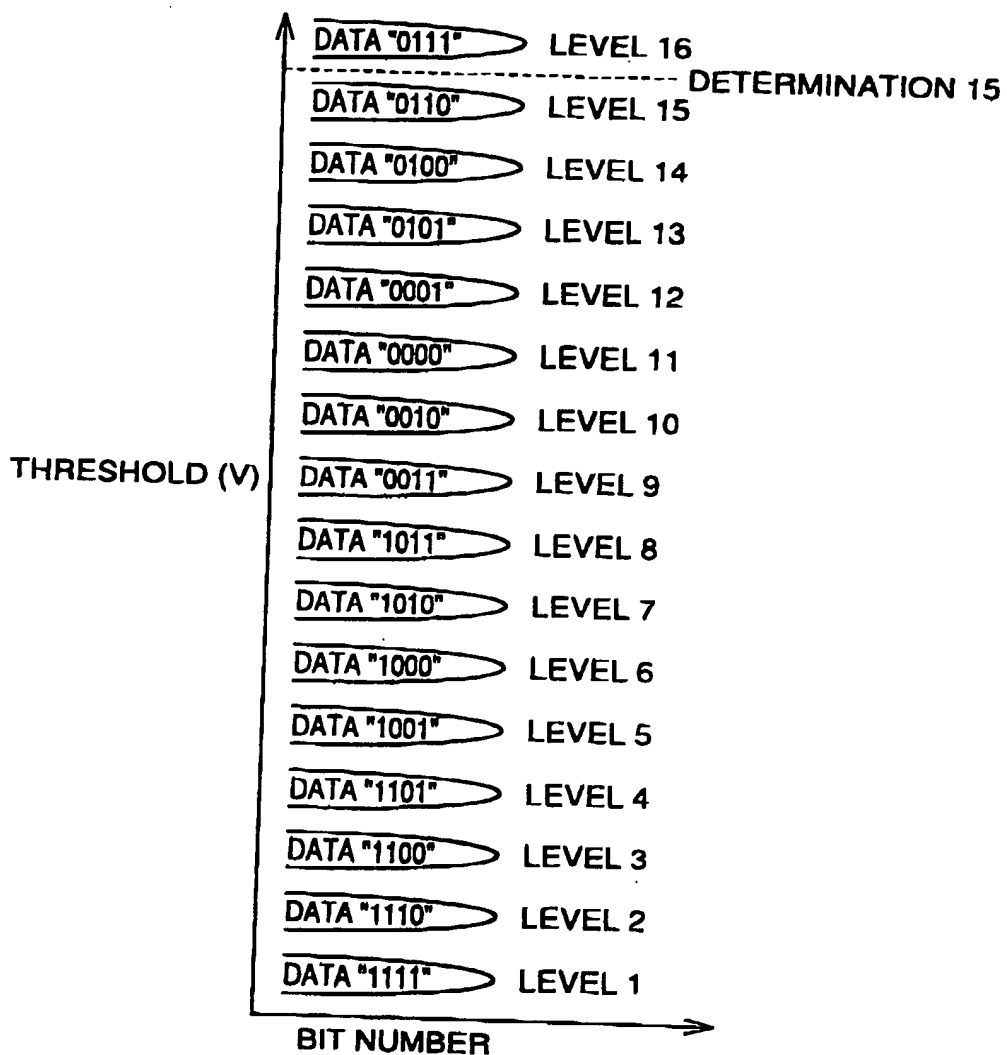
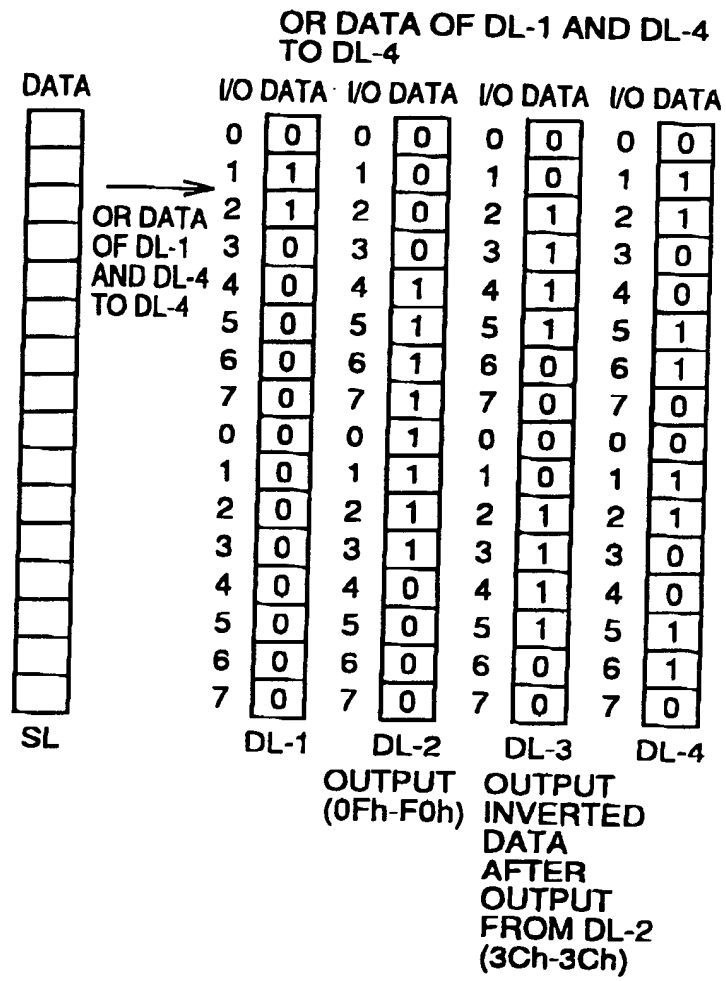
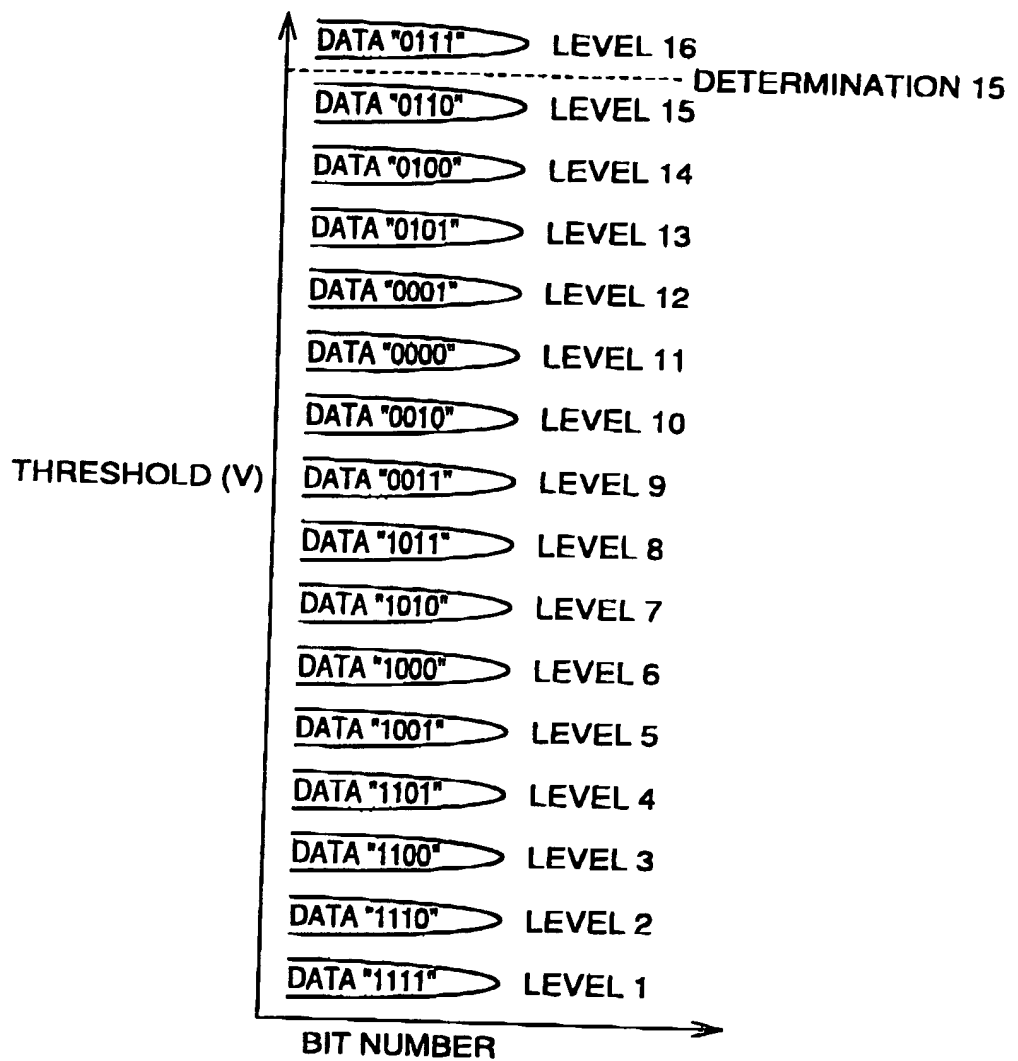


FIG.80



DL-1 DL-2 DL-3 DL-4

FIG. 81



**FIG.82**

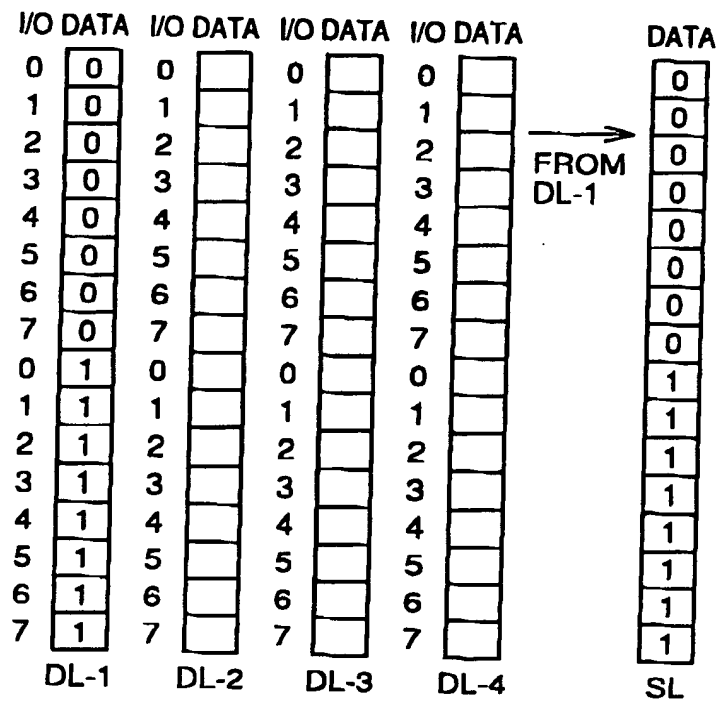
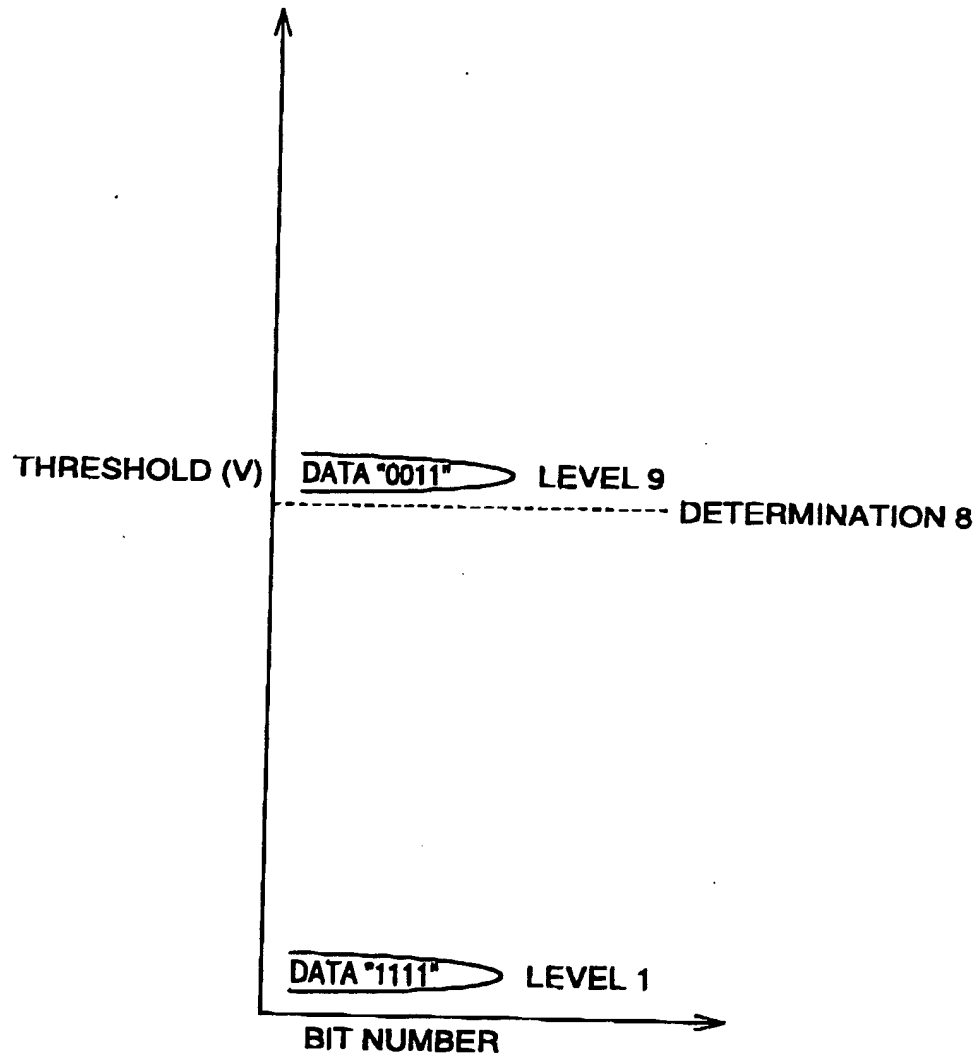


FIG.83



**FIG.84**

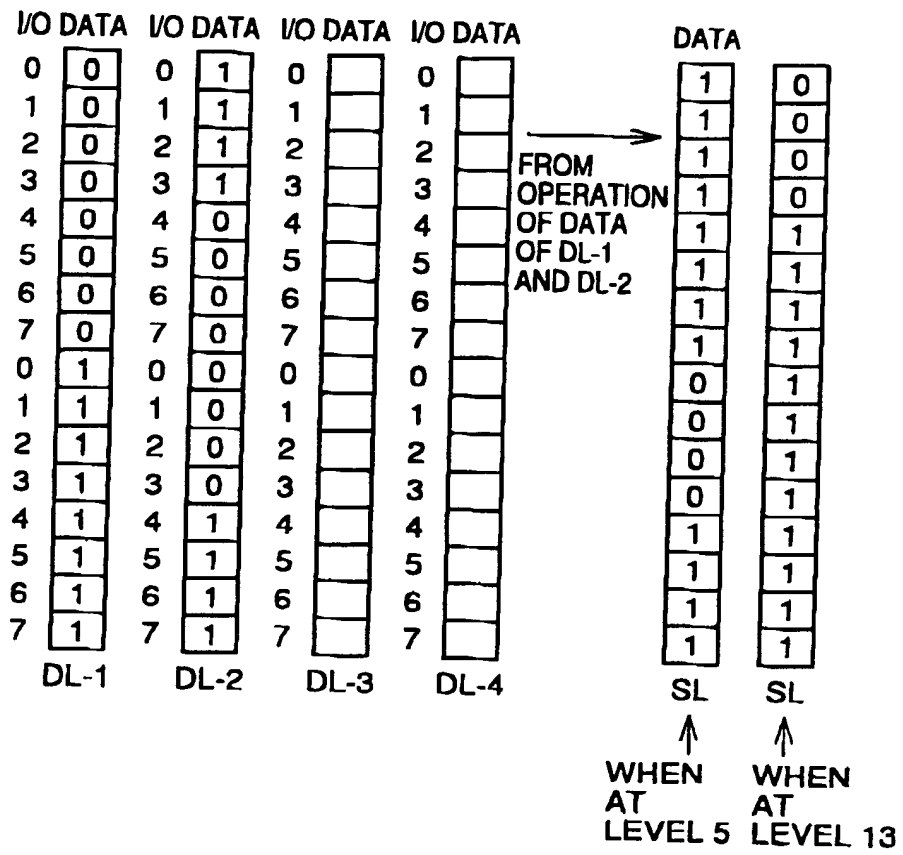
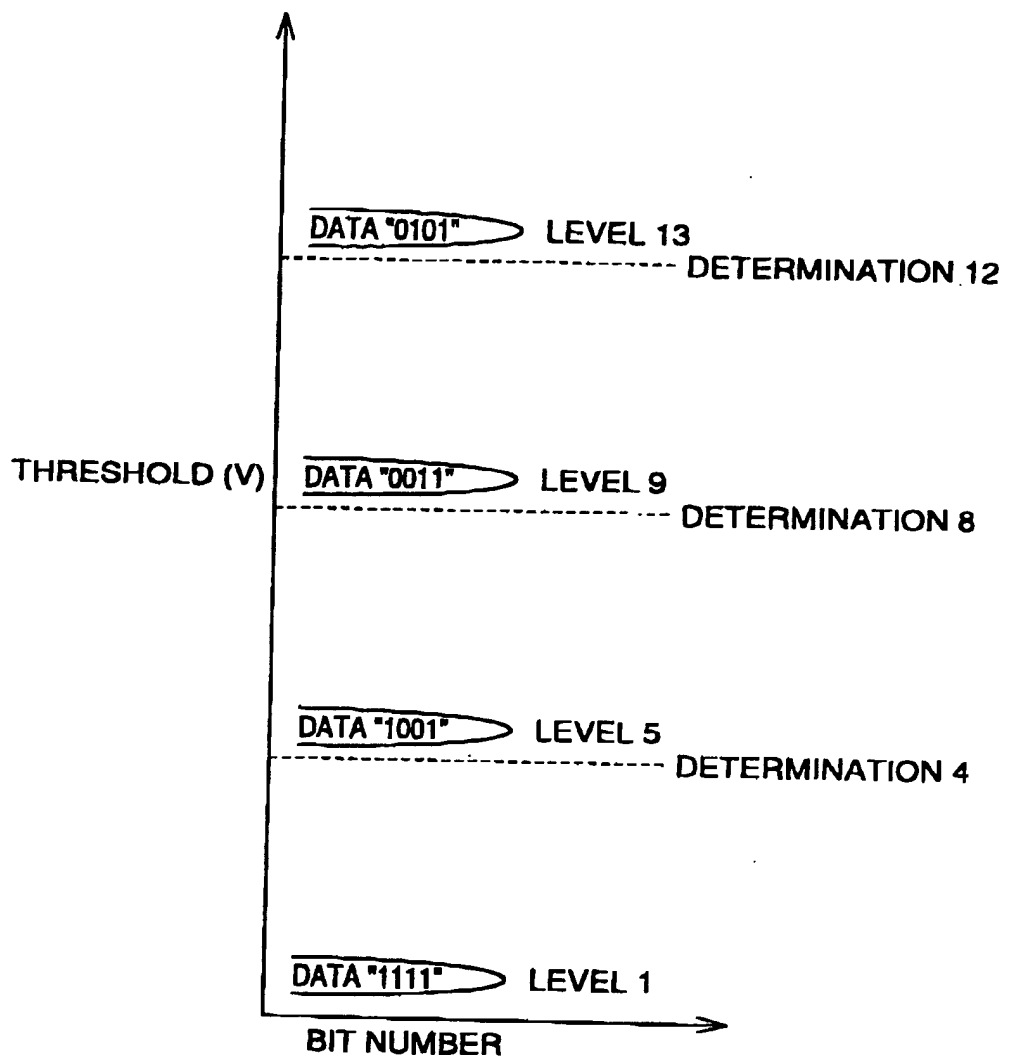
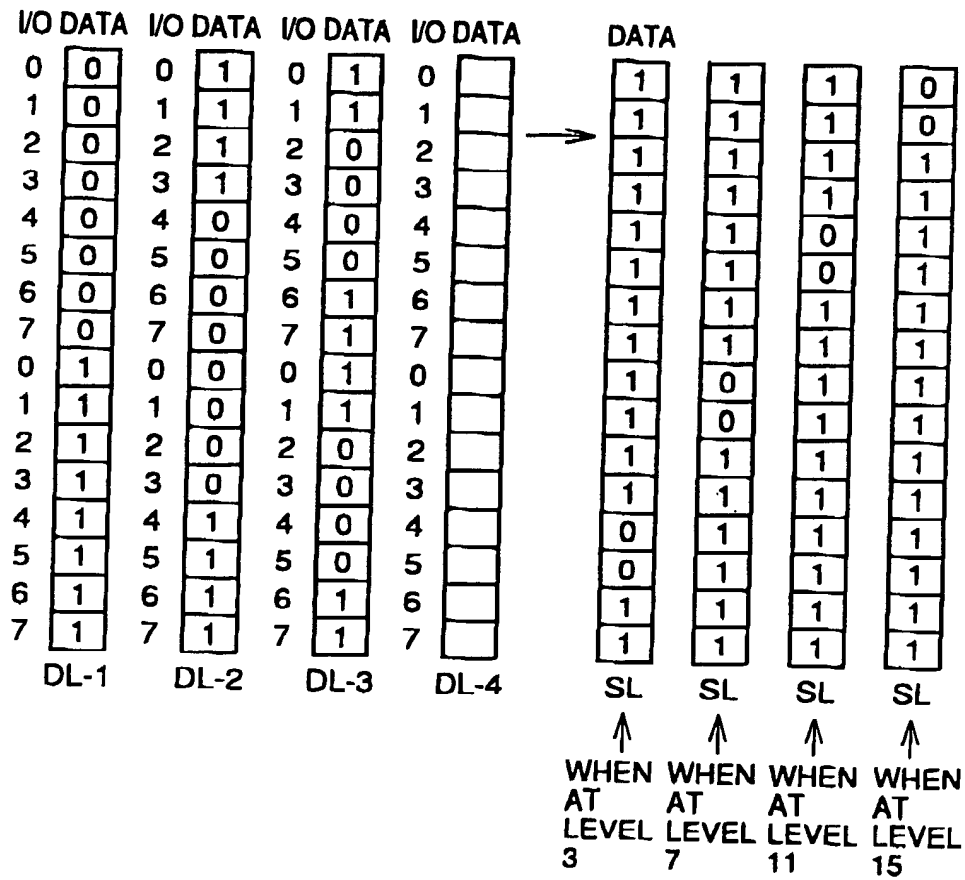


FIG.85



650327-460450

FIG.86



652227 26459460

FIG.87

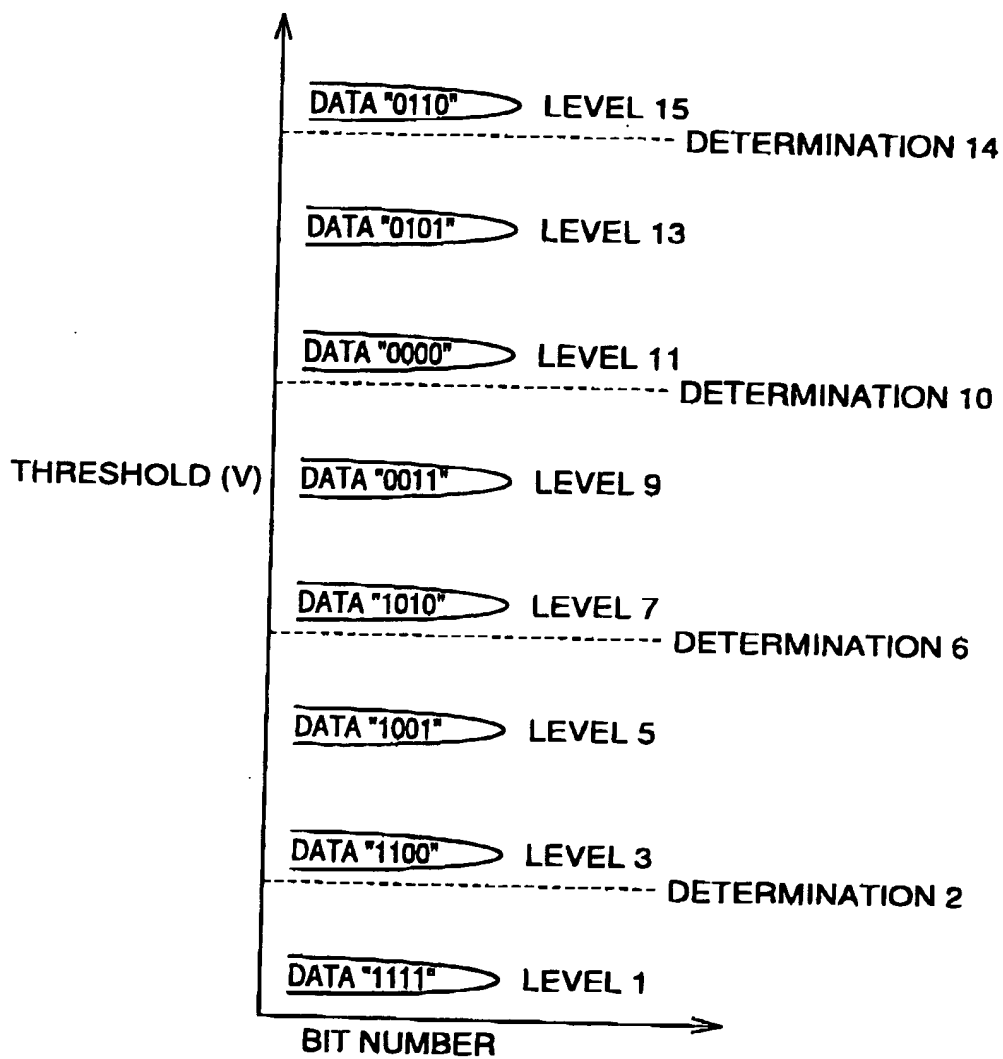


FIG.88

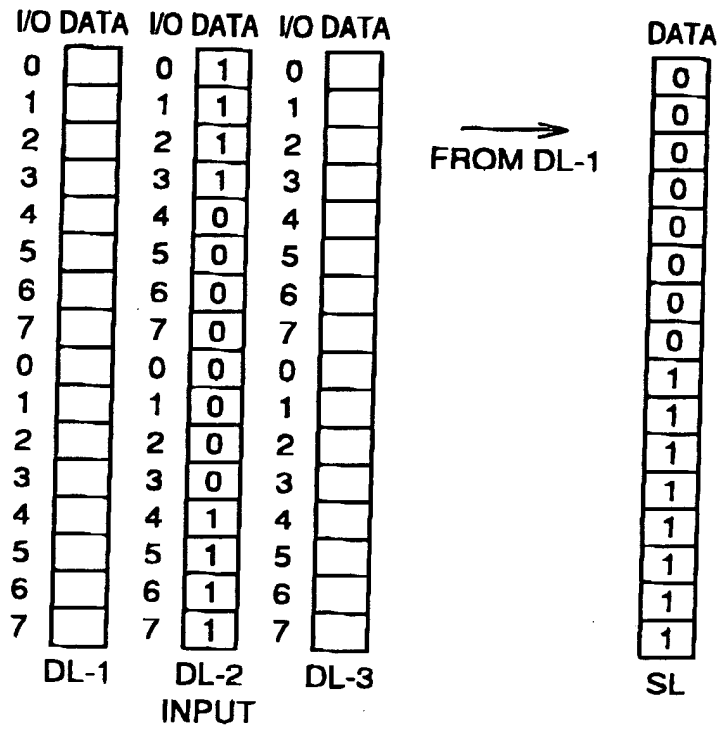
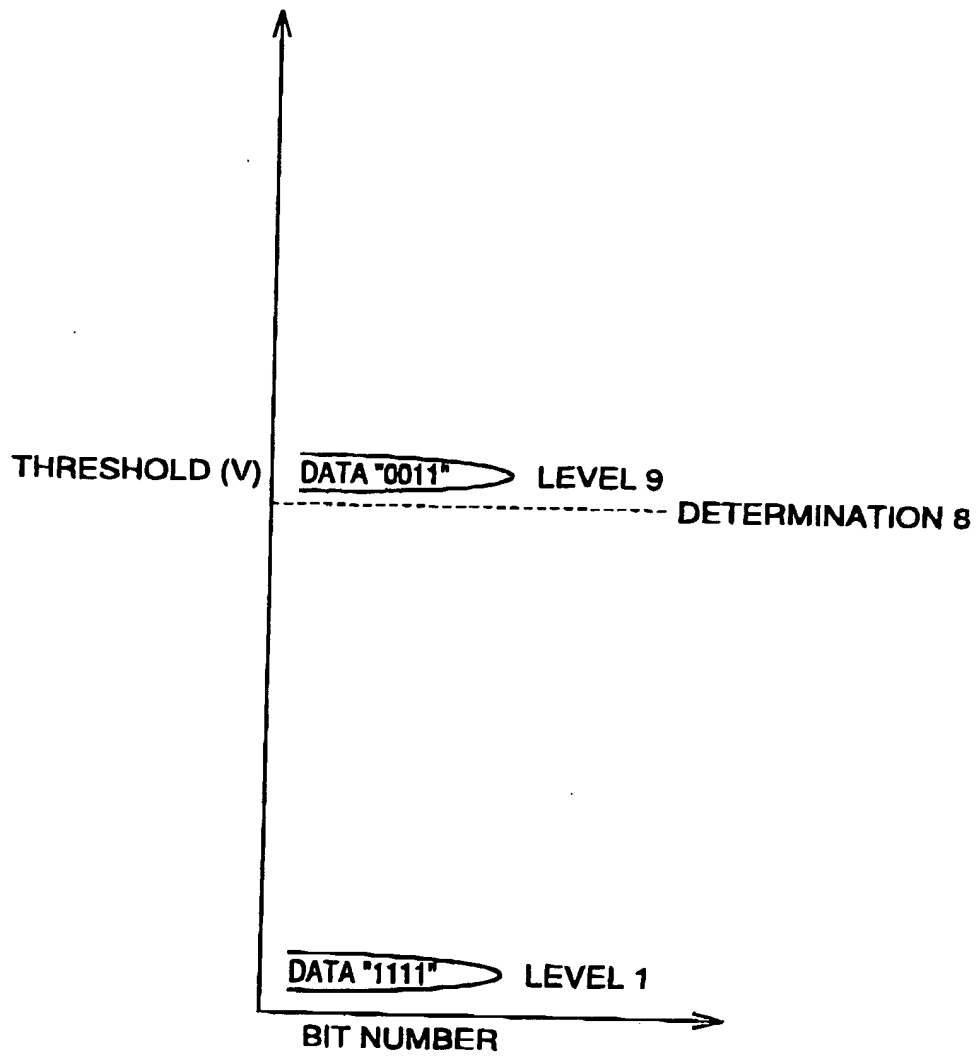


FIG.89



052212P 46469460

FIG.90

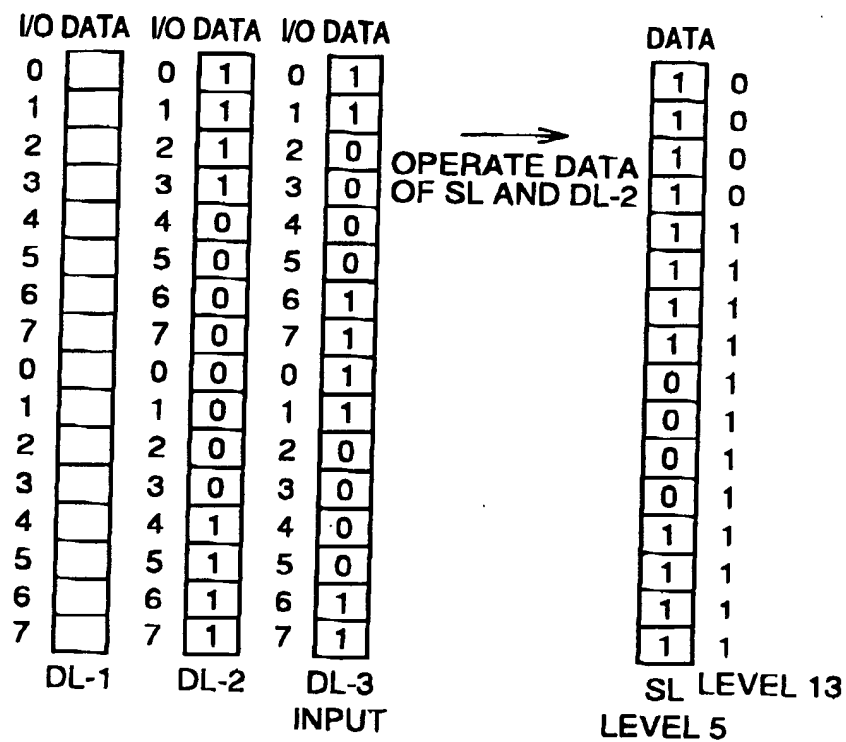
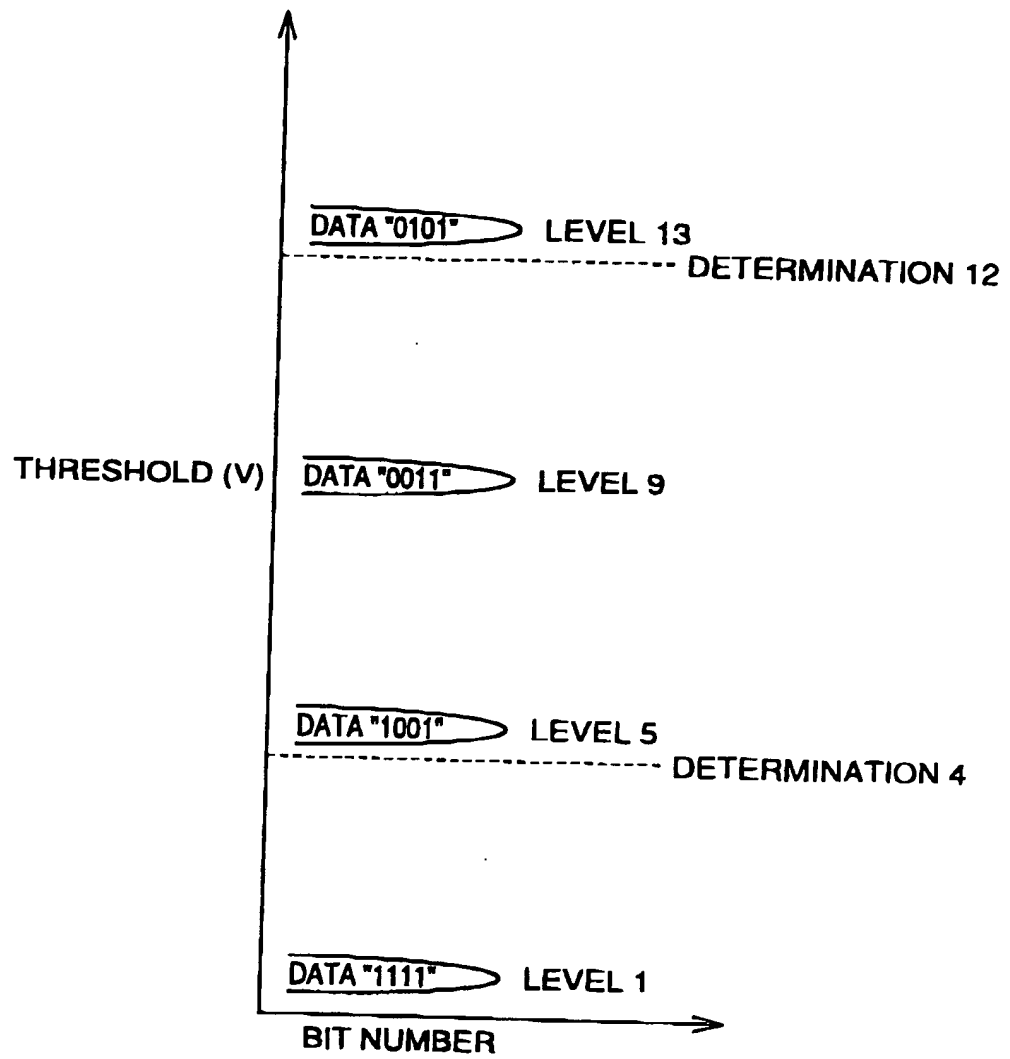
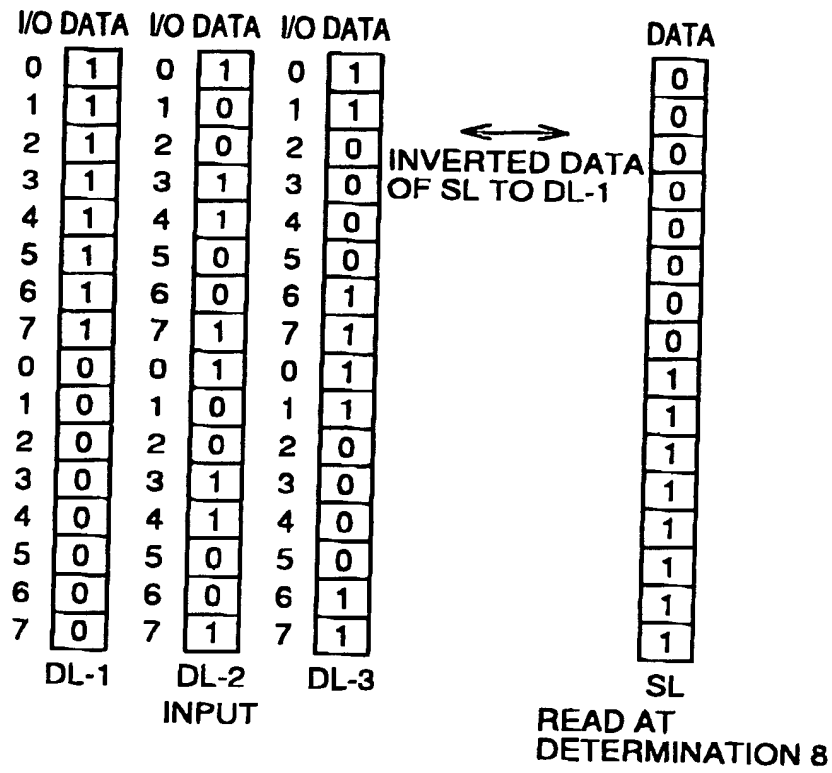


FIG.91



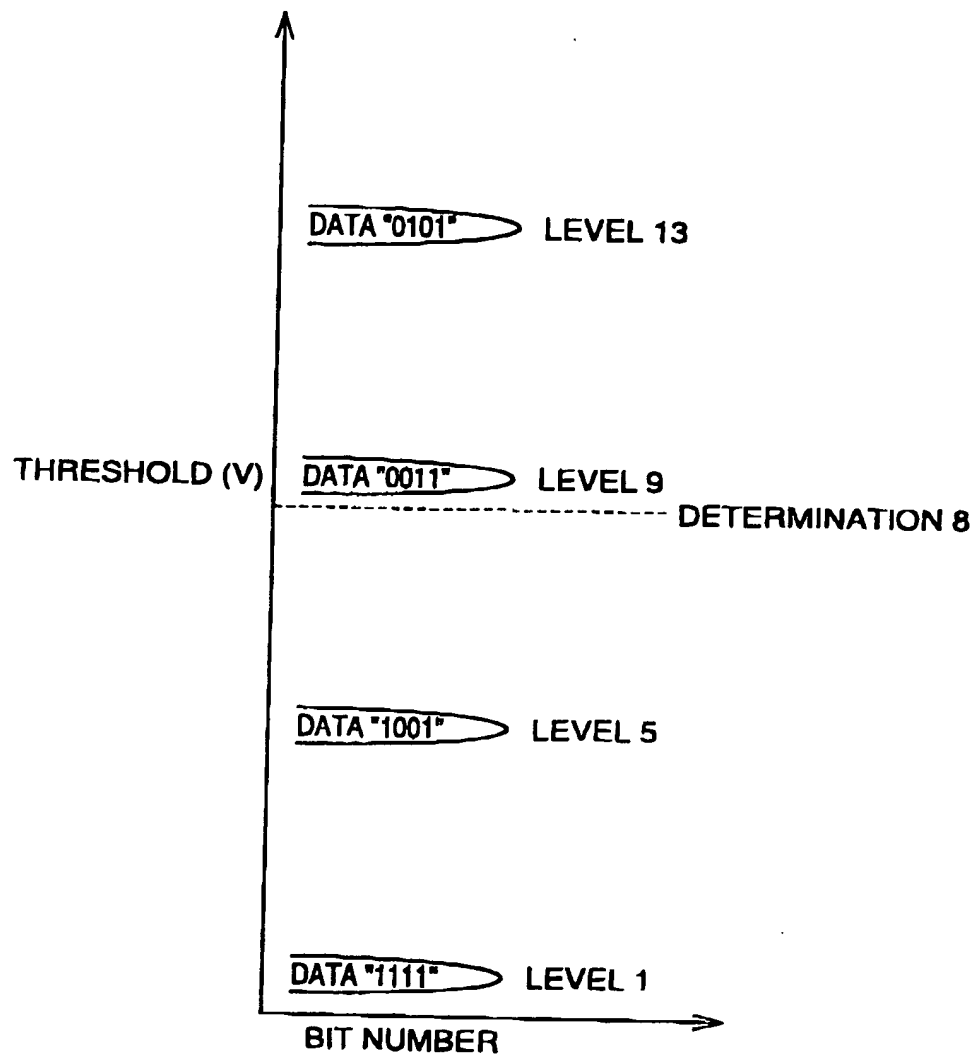
652227 26469460

FIG.92



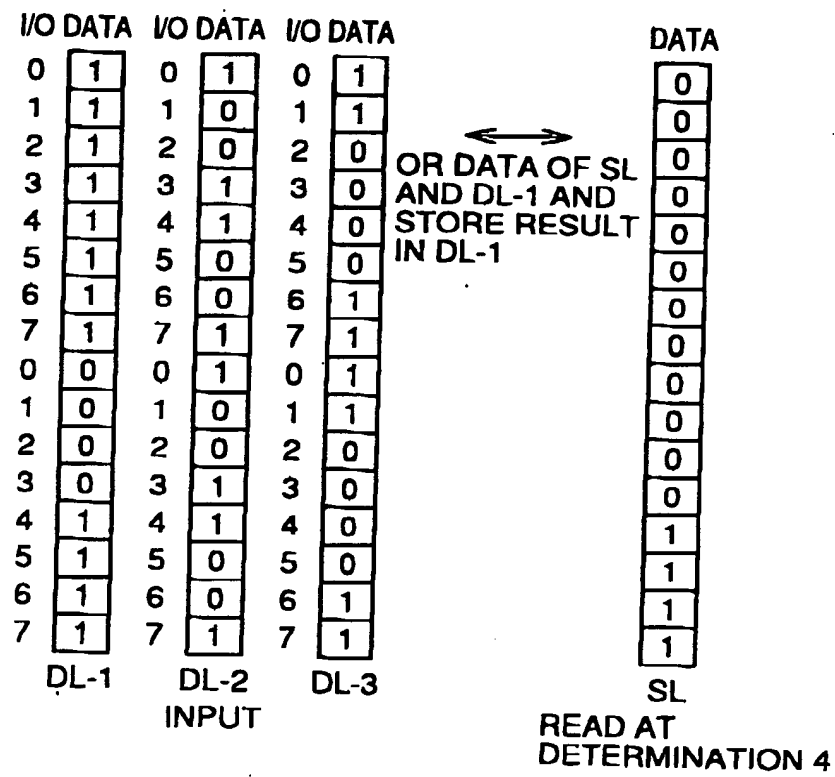
6523237 46469460

FIG.93



09469497 12299

**FIG.94**



66222T 26459460

FIG.95

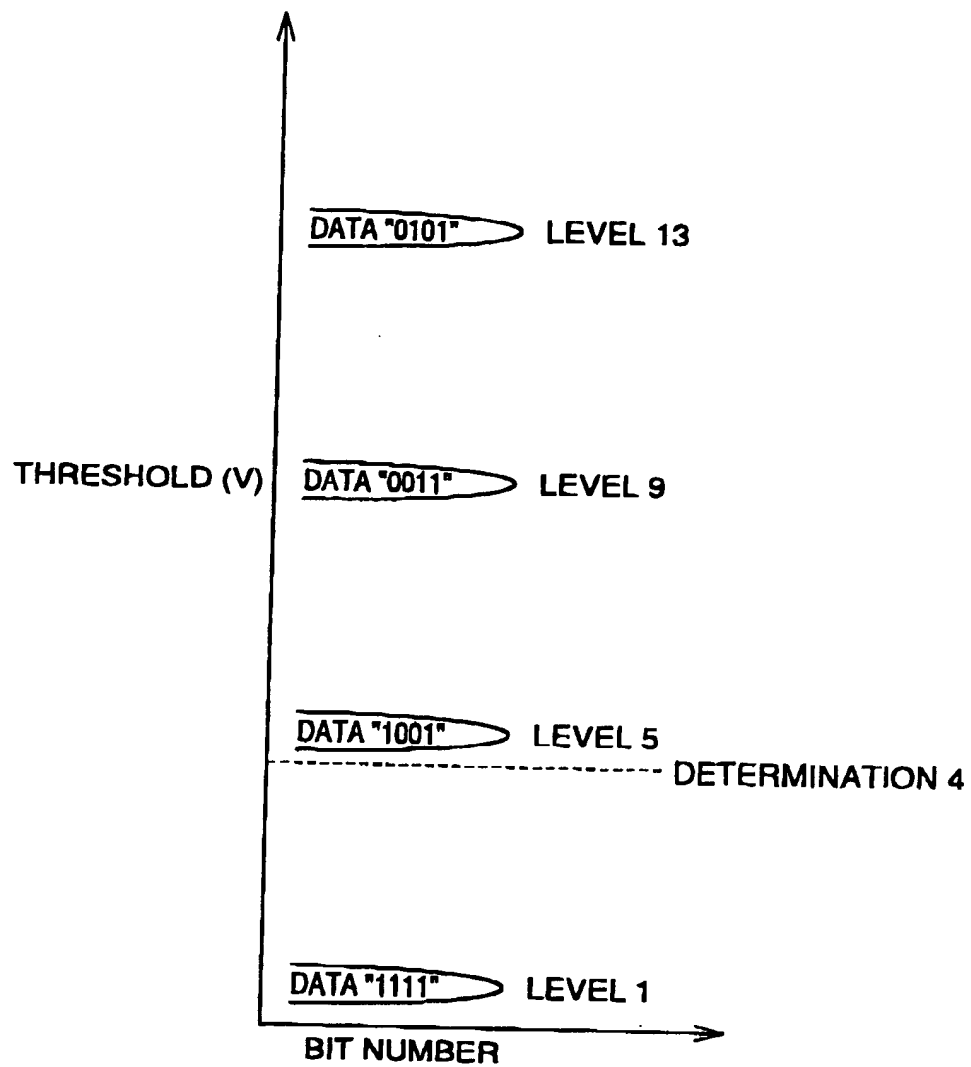


FIG.96

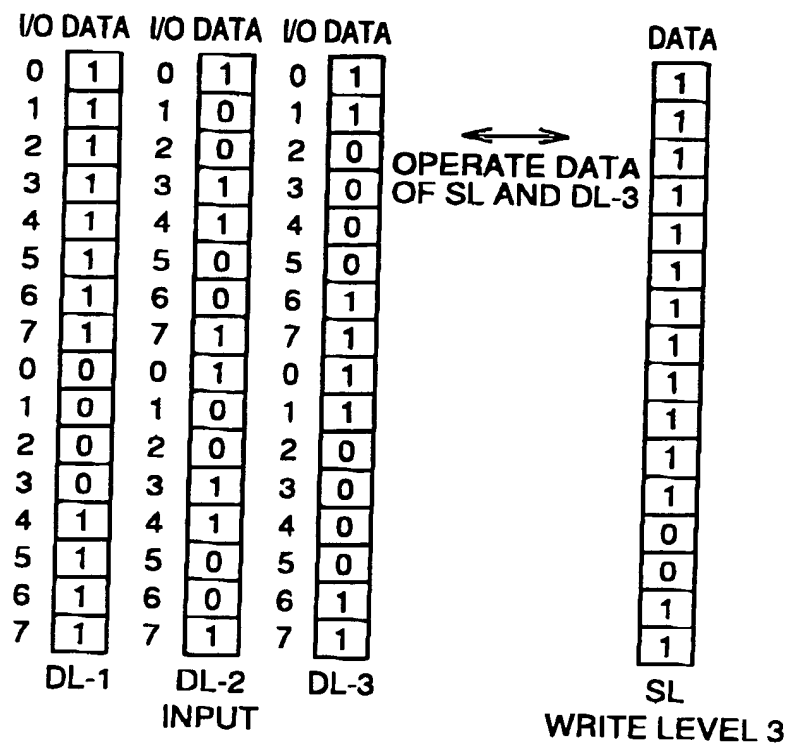
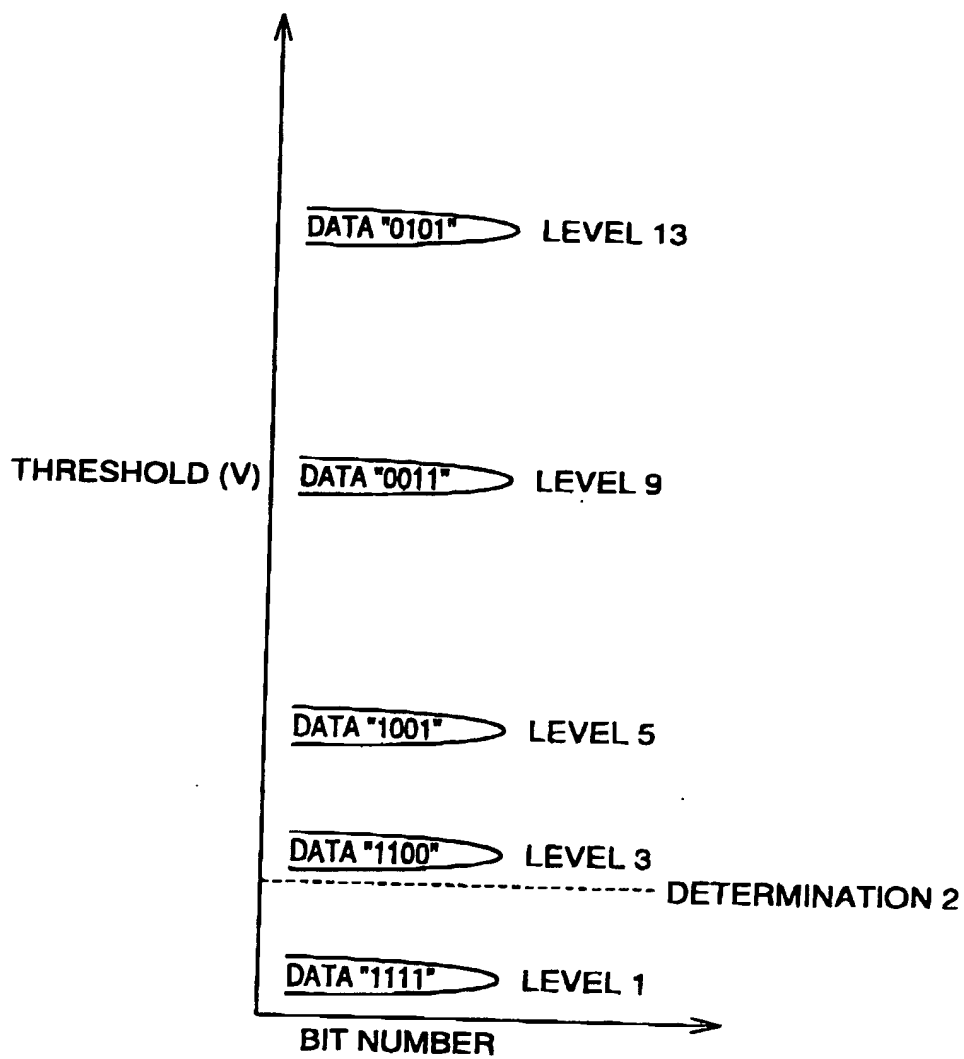


FIG.97



552221 26459460

FIG.98

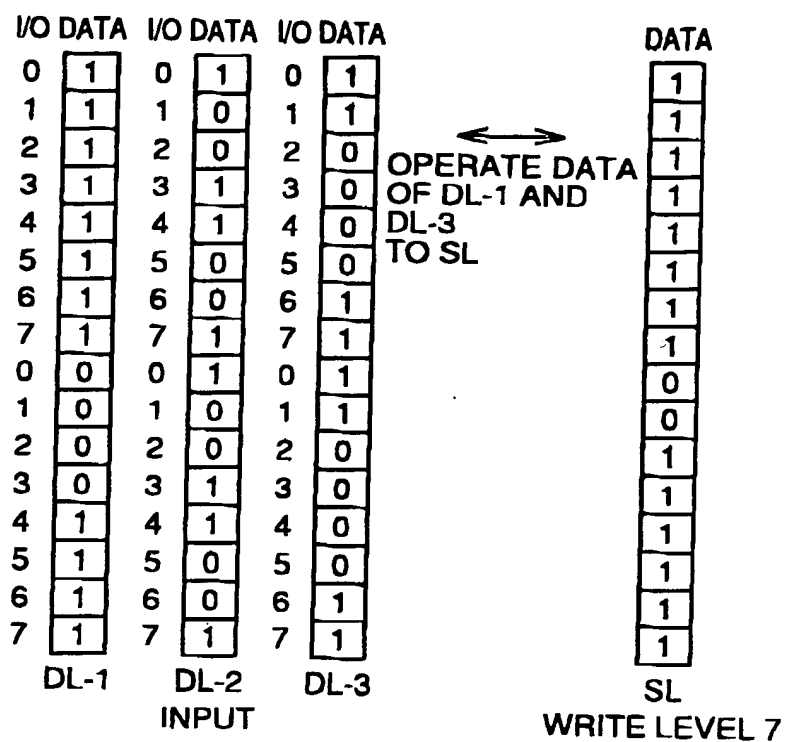
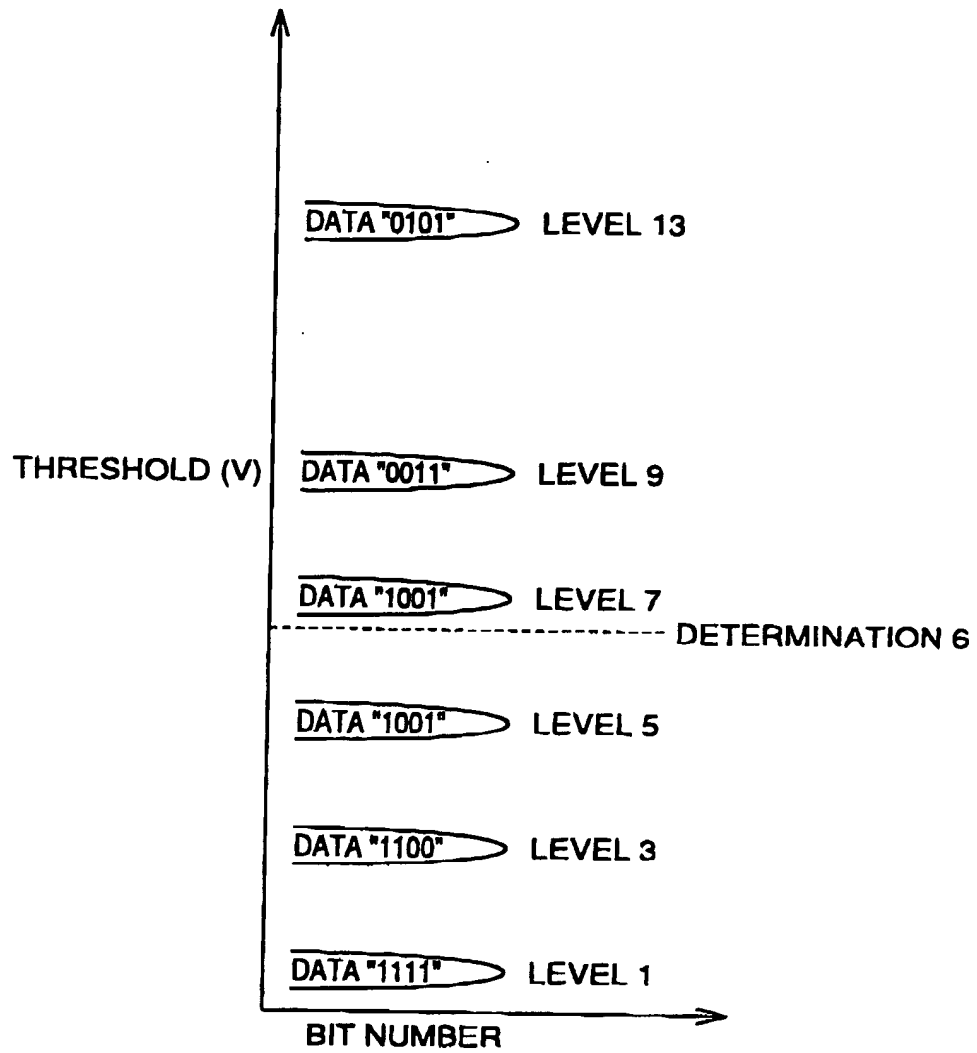


FIG.99



0469450 230322Z

**FIG. 100**

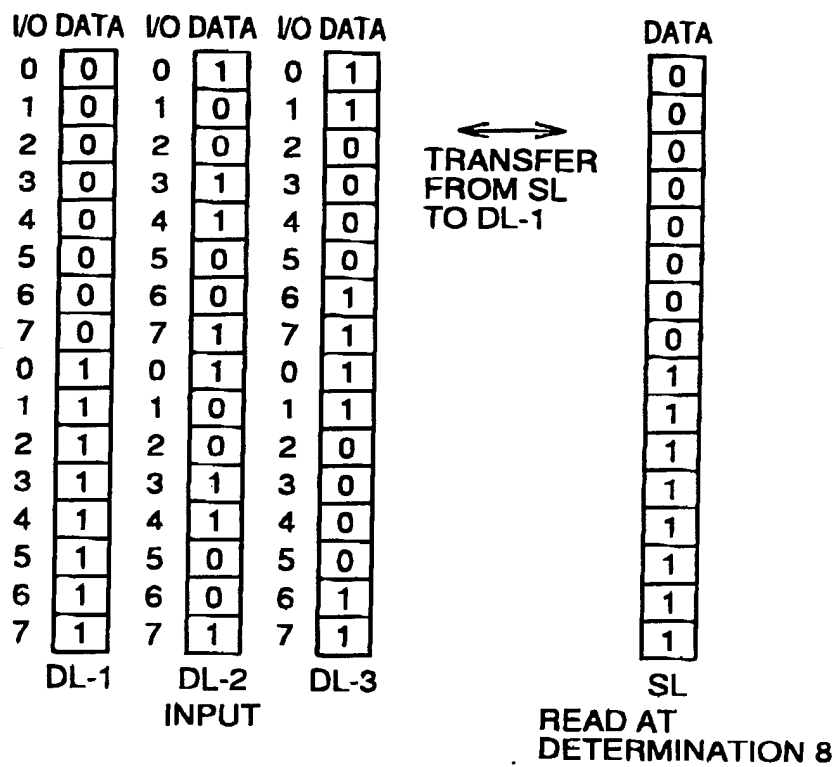
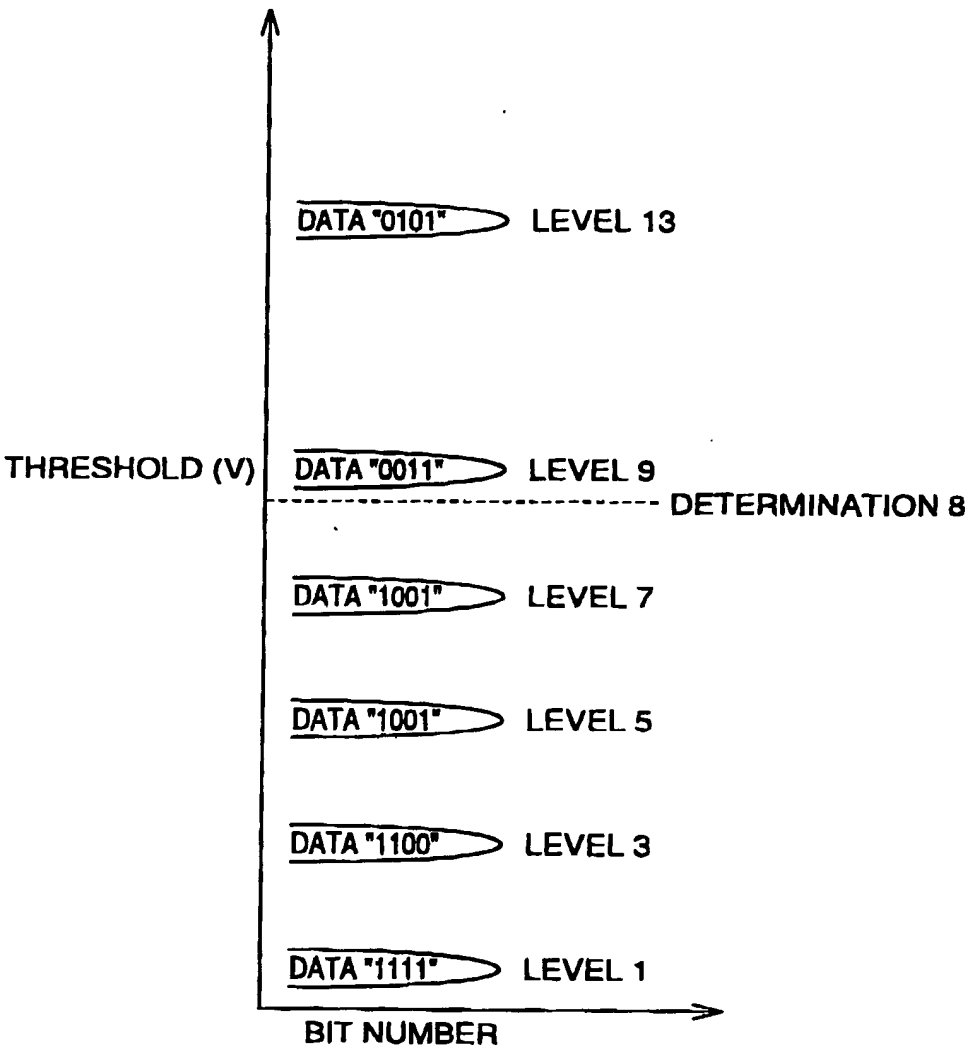
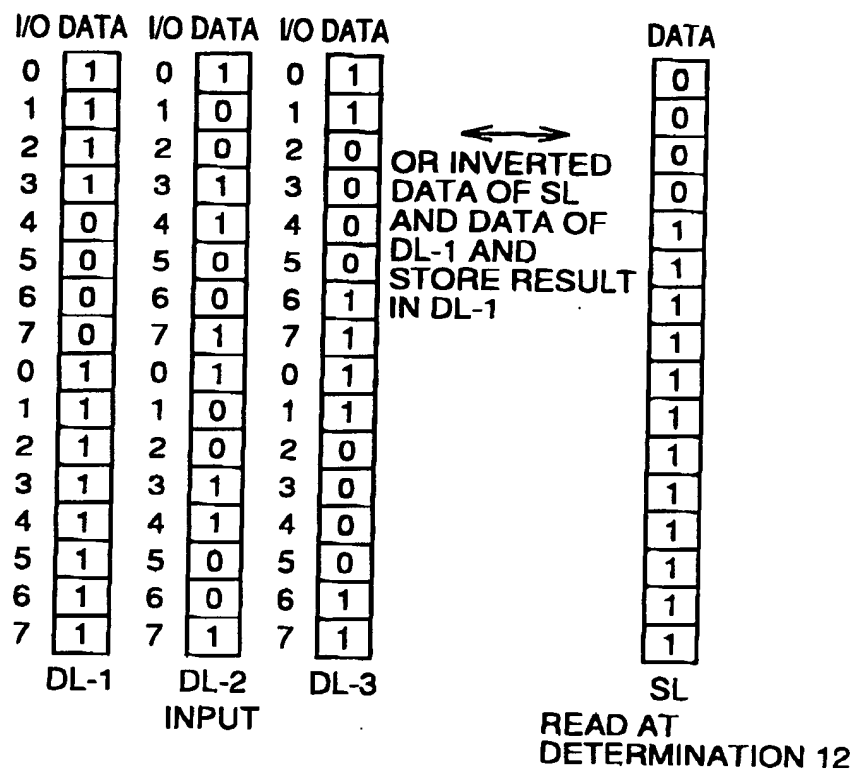


FIG. 101



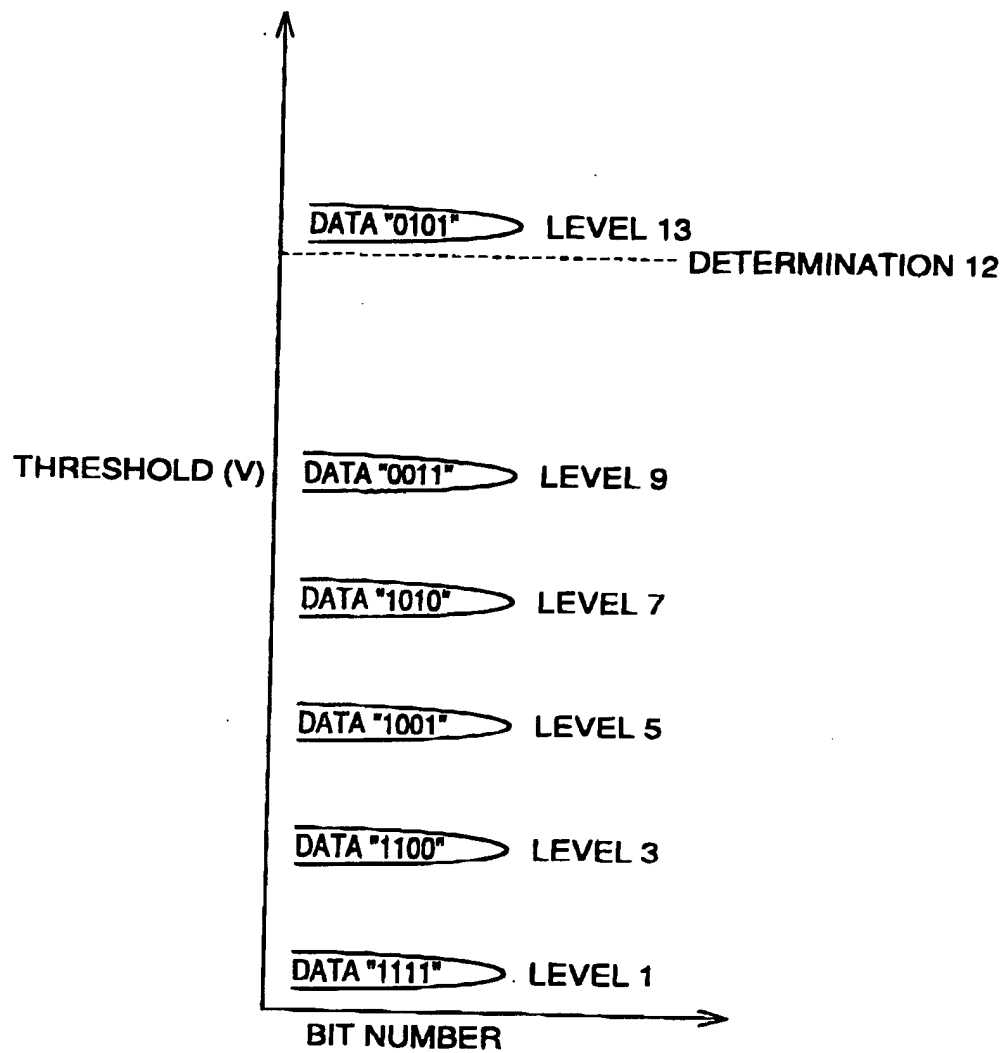
552221 46469460

FIG. 102



662237-26469460

FIG. 103



662231 25469460

FIG.104

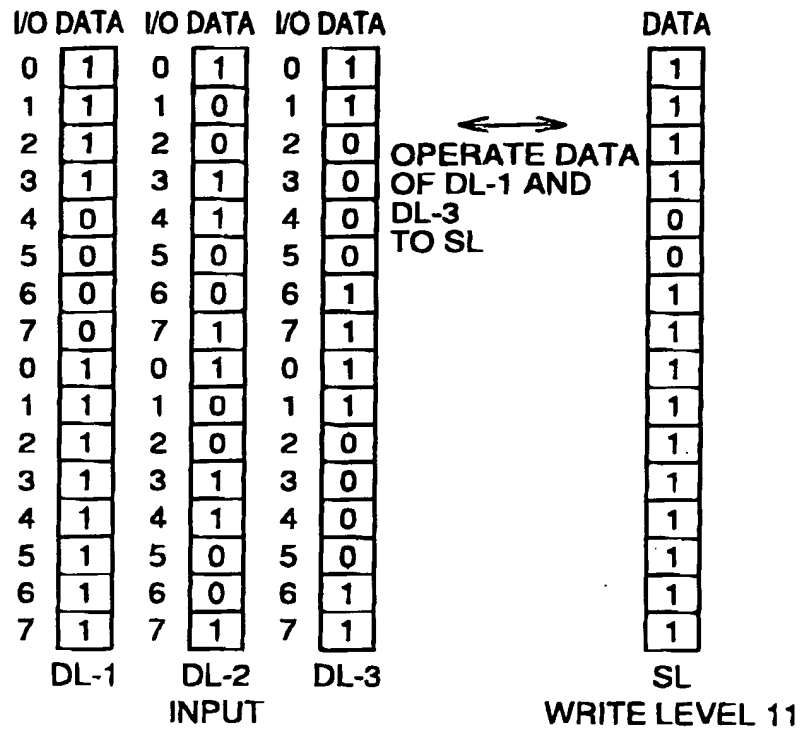
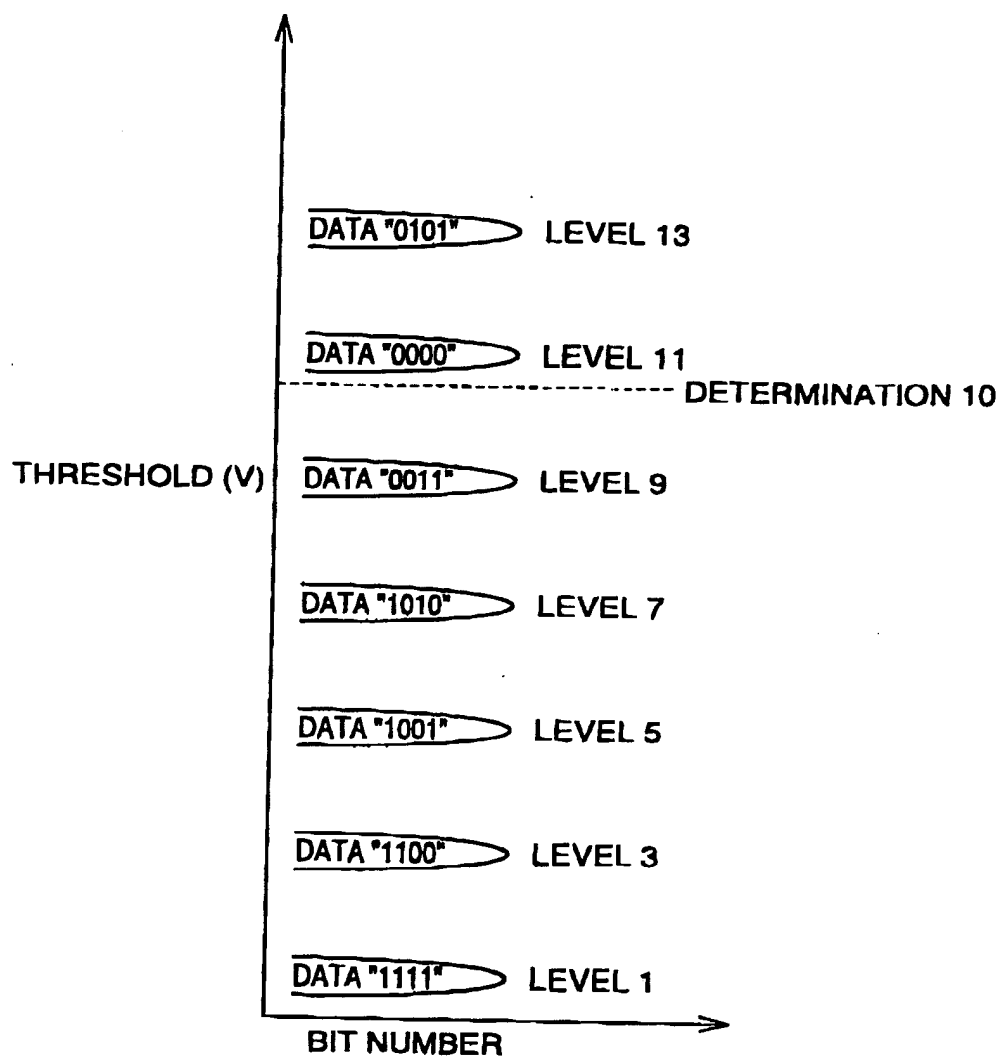
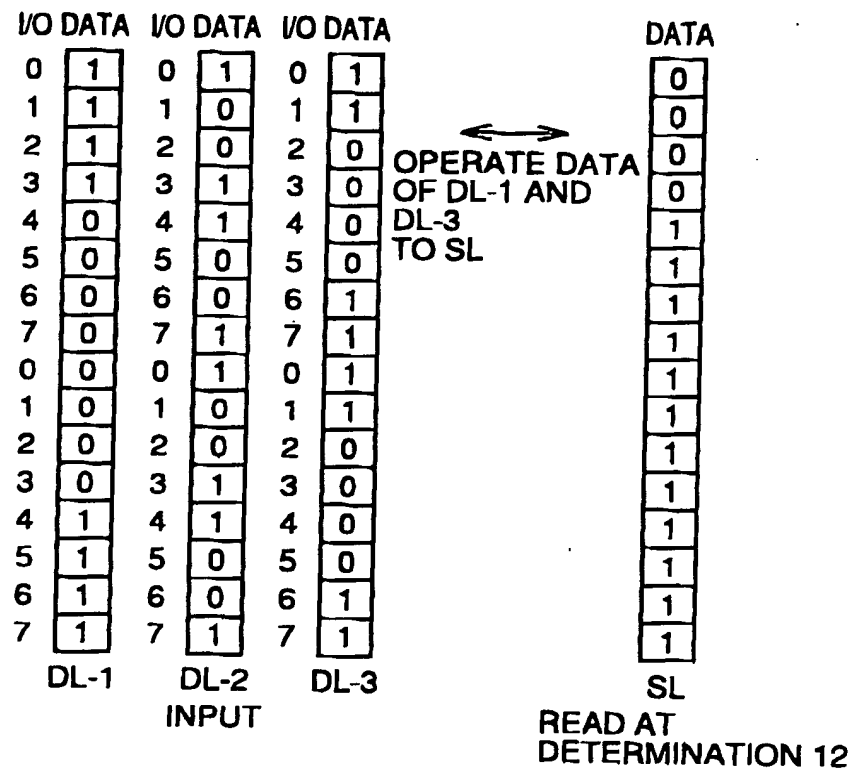


FIG. 105



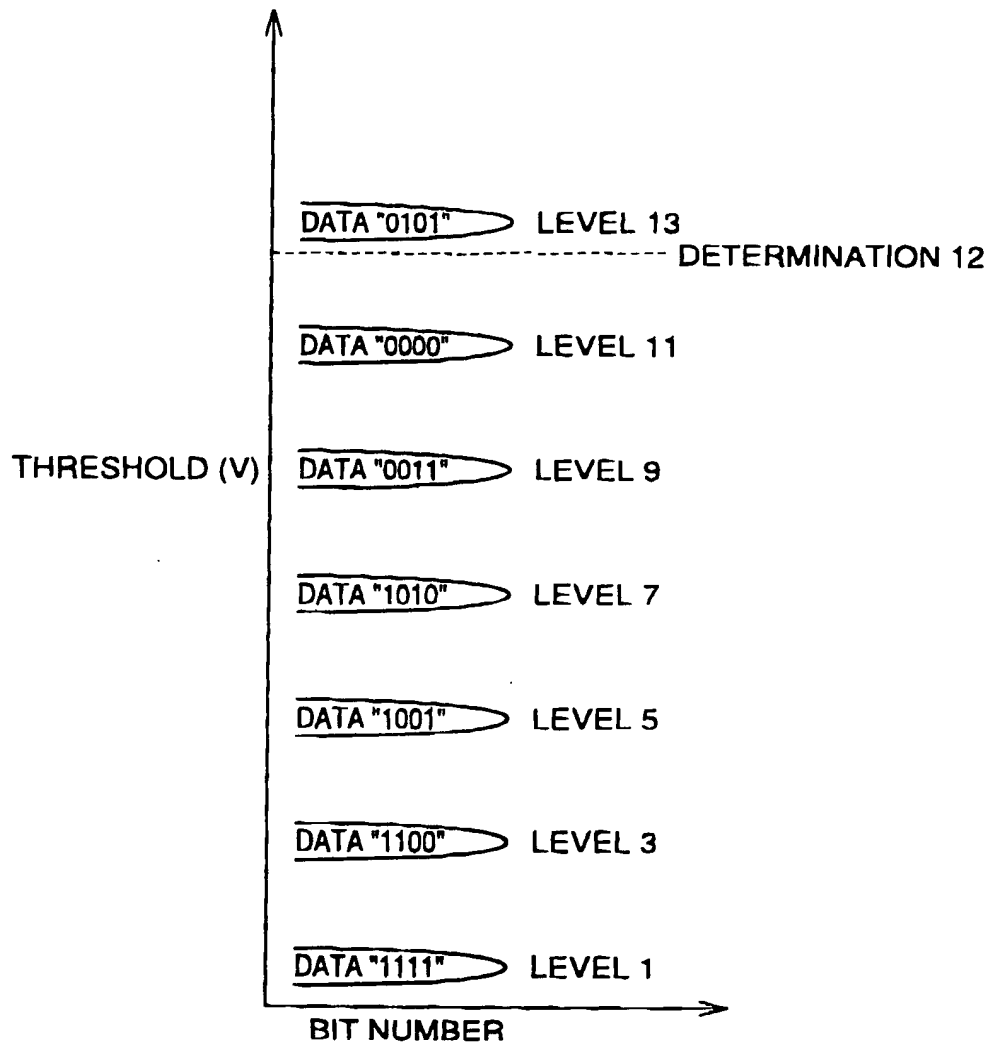
662231 26469150

FIG. 106



662227 46469460

FIG. 107



65233 26469

FIG. 108

I/O DATA	I/O DATA	I/O DATA
0	0	0
1	1	1
2	0	0
3	1	0
4	1	0
5	0	0
6	0	1
7	1	1
0	1	0
1	0	1
2	0	0
3	1	0
4	1	0
5	0	0
6	0	1
7	1	1
DL-1	DL-2	DL-3
	INPUT	

DATA
0
0
1
1
1
1
1
1
1
1
1
1
1
1
SL
WRITE LEVEL 15

662222T 26469460

FIG.109

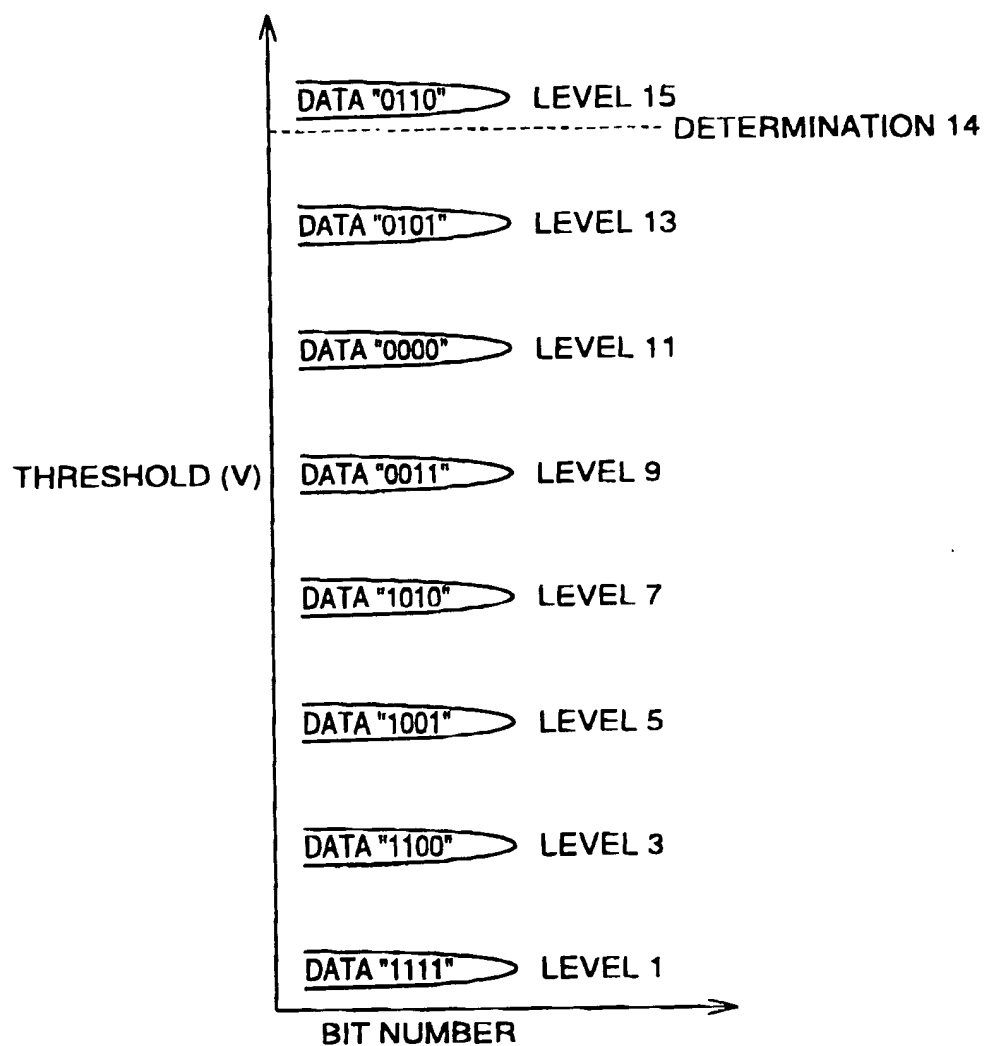
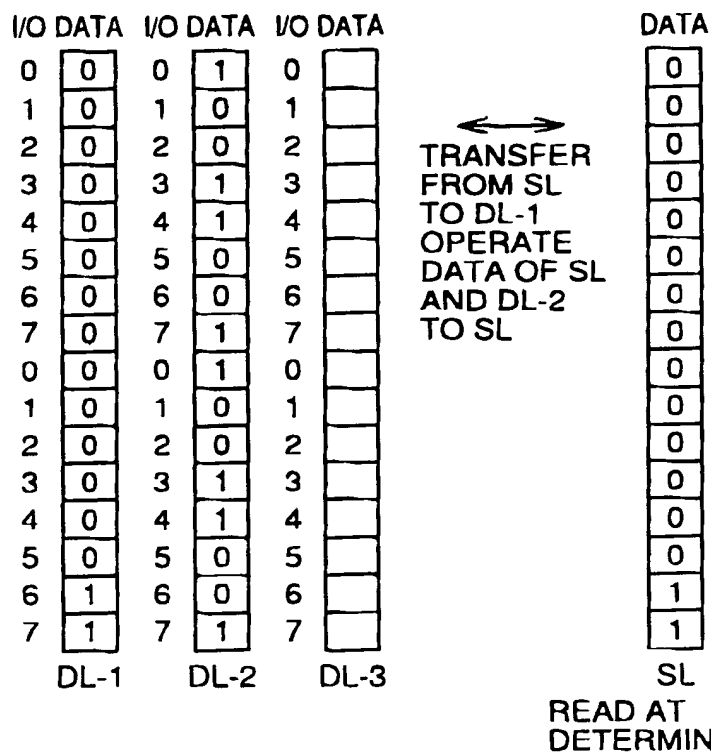


FIG.110



662227 25469460

FIG.111

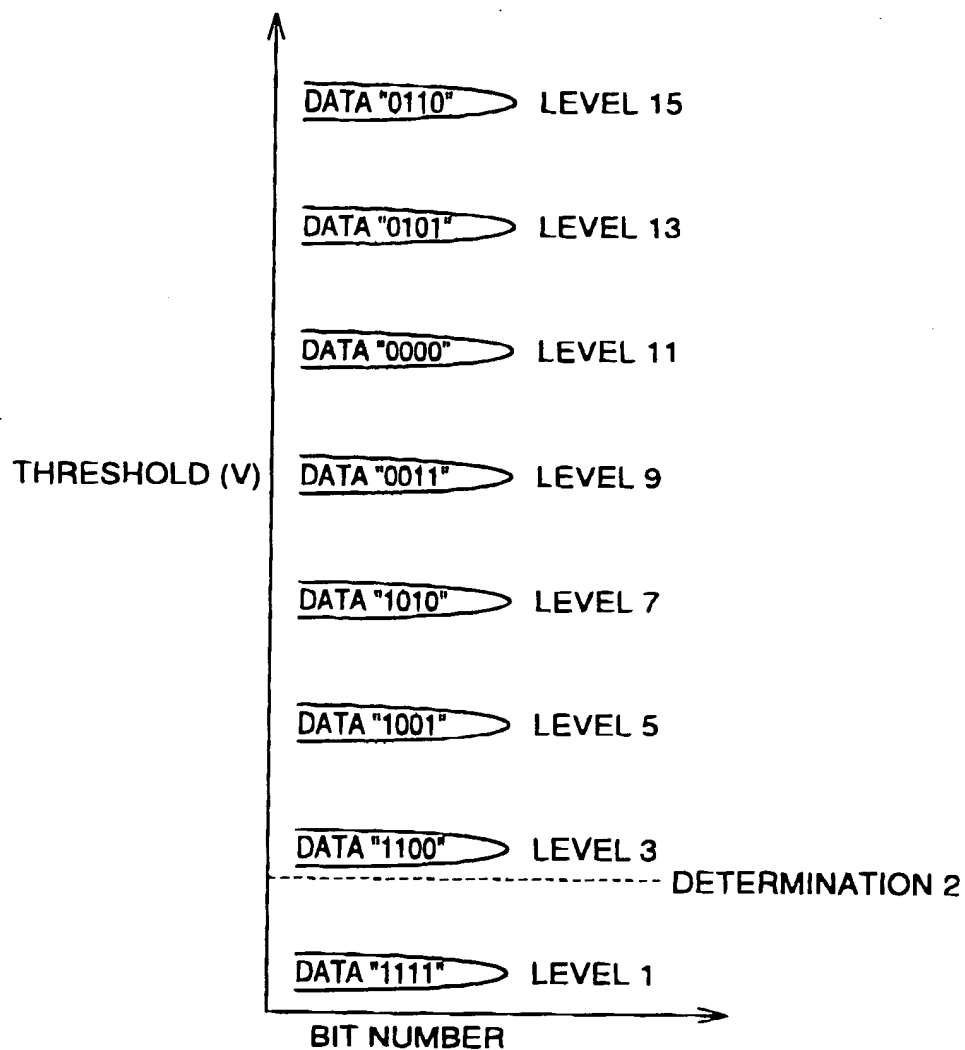
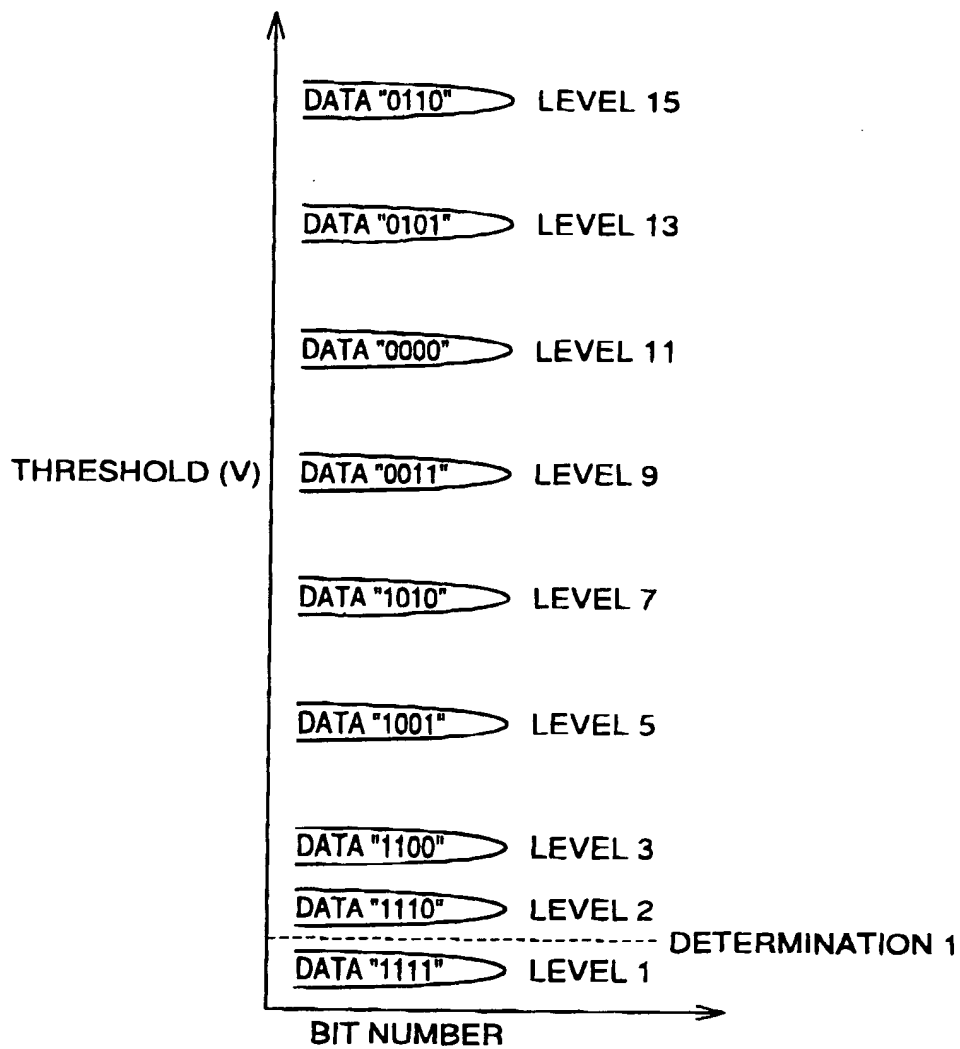


FIG.112

I/O DATA	I/O DATA	I/O DATA
0 0	0 1	0
1 0	1 0	1
2 0	2 0	2
3 0	3 1	3
4 0	4 1	4
5 0	5 0	5
6 0	6 0	6
7 0	7 1	7
0 0	0 1	0
1 0	1 0	1
2 0	2 0	2
3 0	3 1	3
4 0	4 1	4
5 0	5 0	5
6 1	6 0	6
7 1	7 1	7
DL-1	DL-2	DL-3

DATA
1
1
1
1
1
1
1
1
1
1
1
1
1
0
1
SL
WRITE LEVEL 2

FIG.113



663317 463460

FIG.114

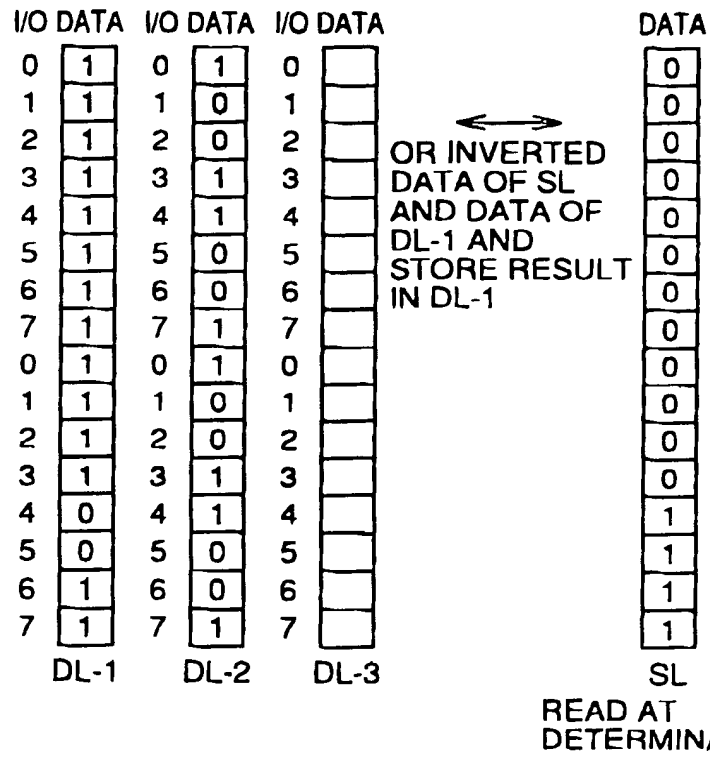
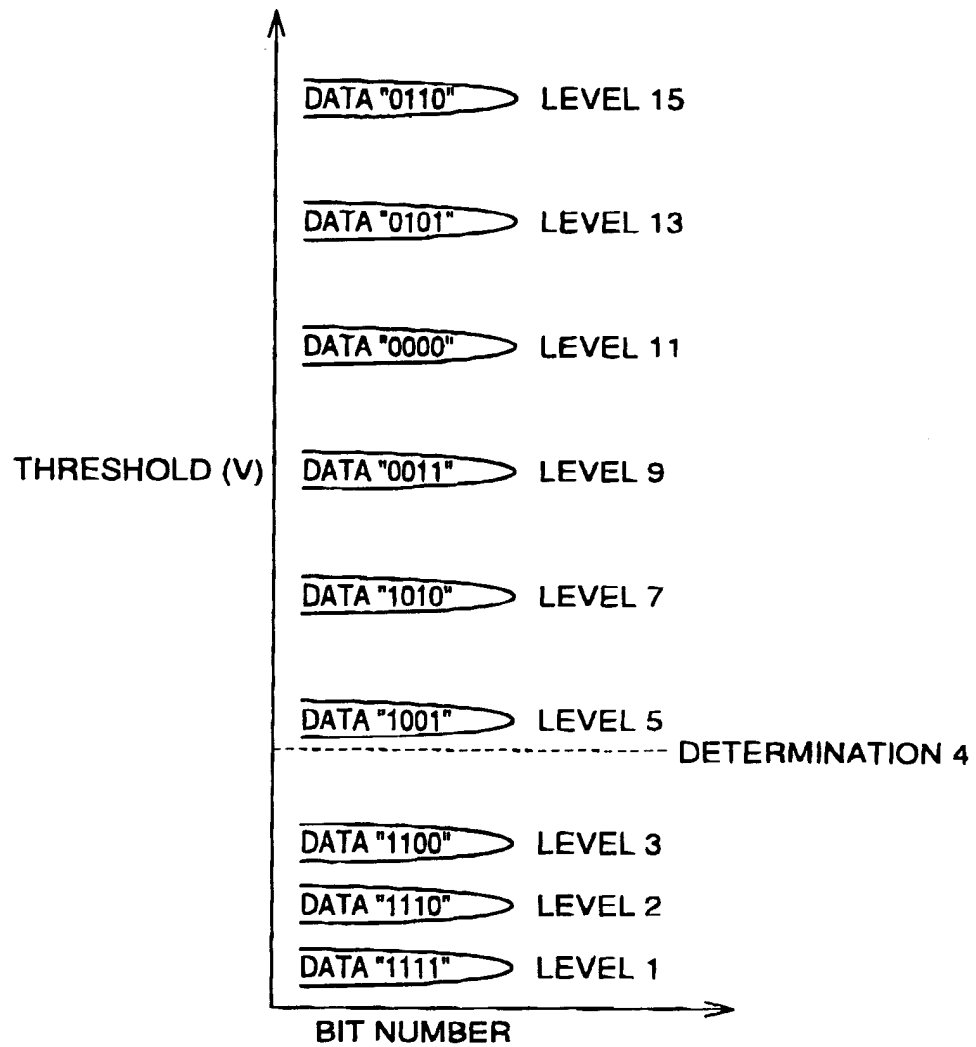


FIG.115



6523231 26463460

FIG. 116

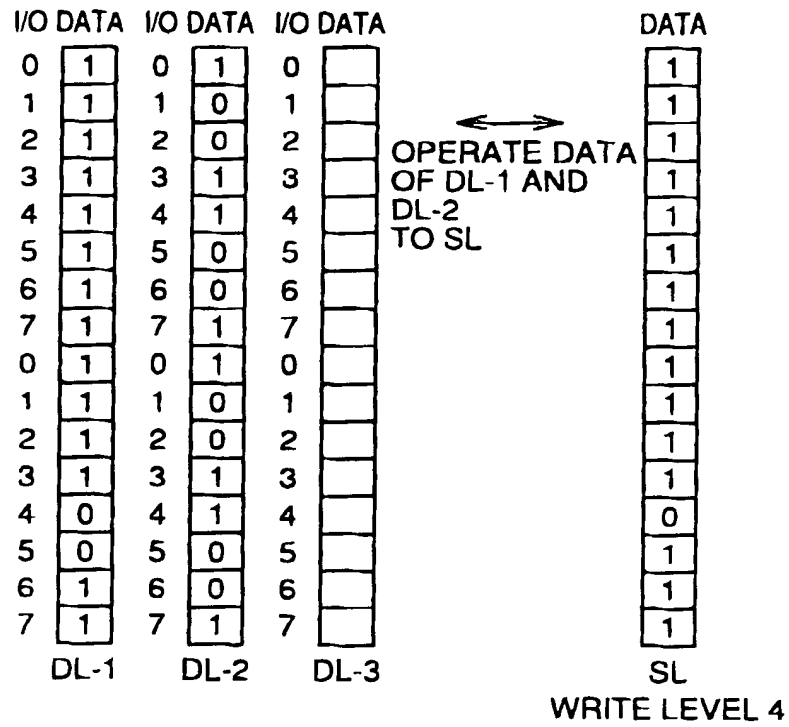
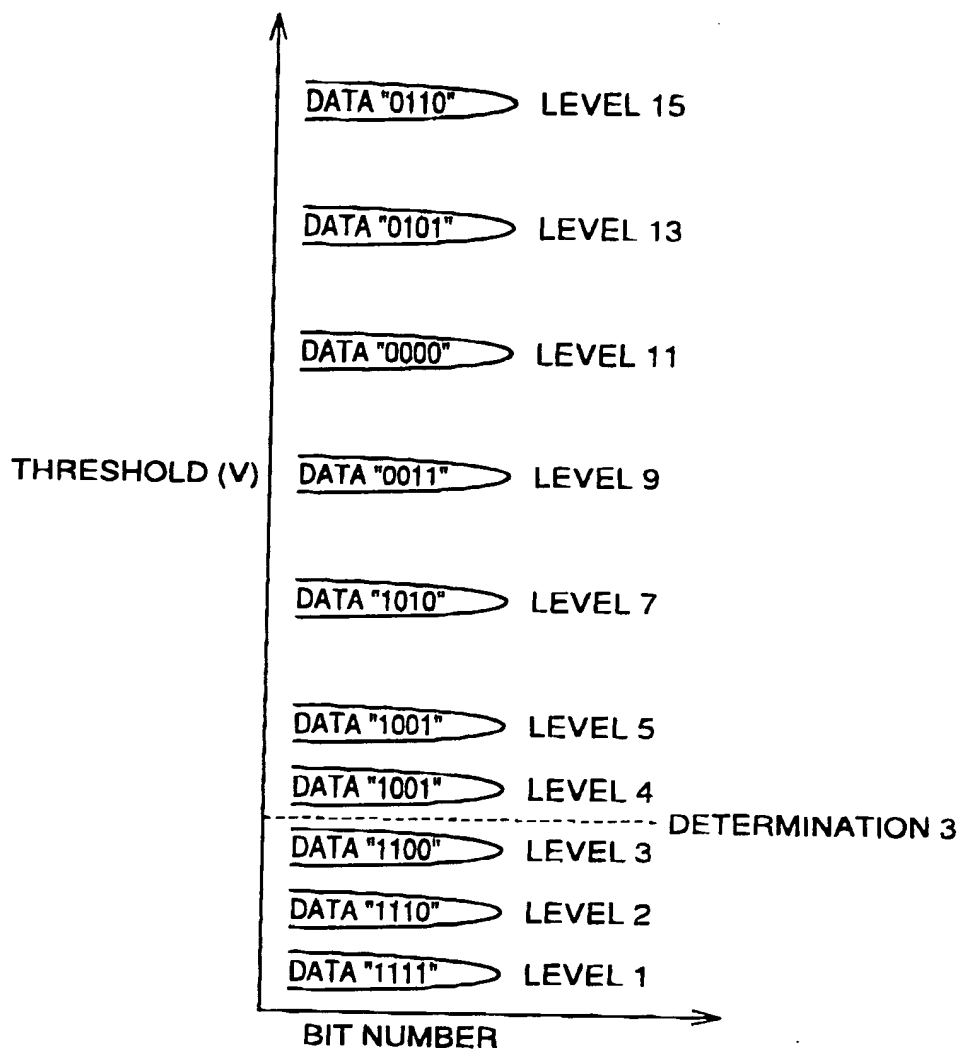


FIG.117

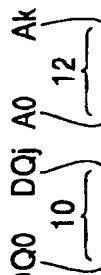


65231T 25469460

FIG. 118

PRIOR ART

DQ0 DQj A0 Ak



8000

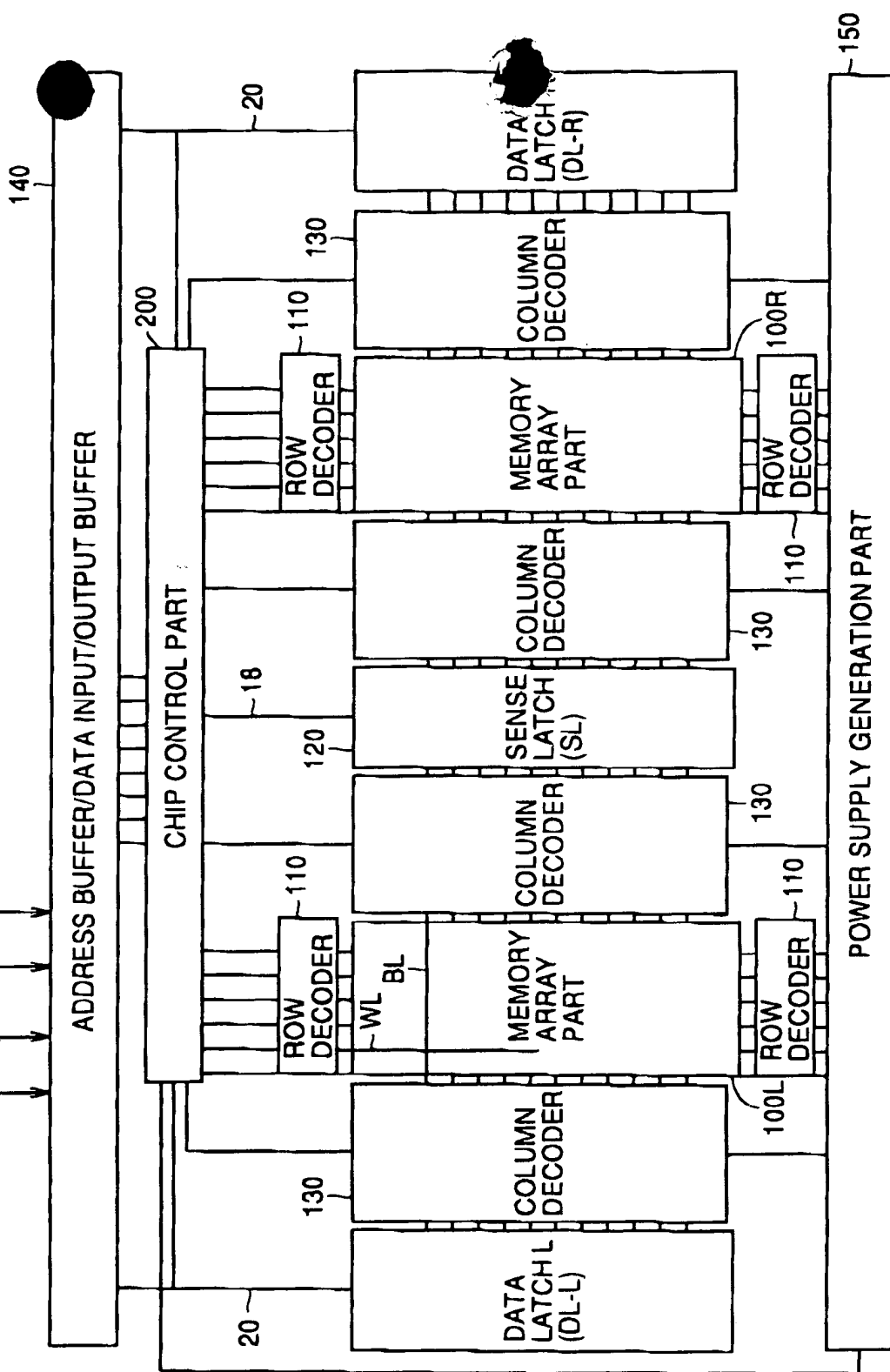


FIG. 119 PRIOR ART

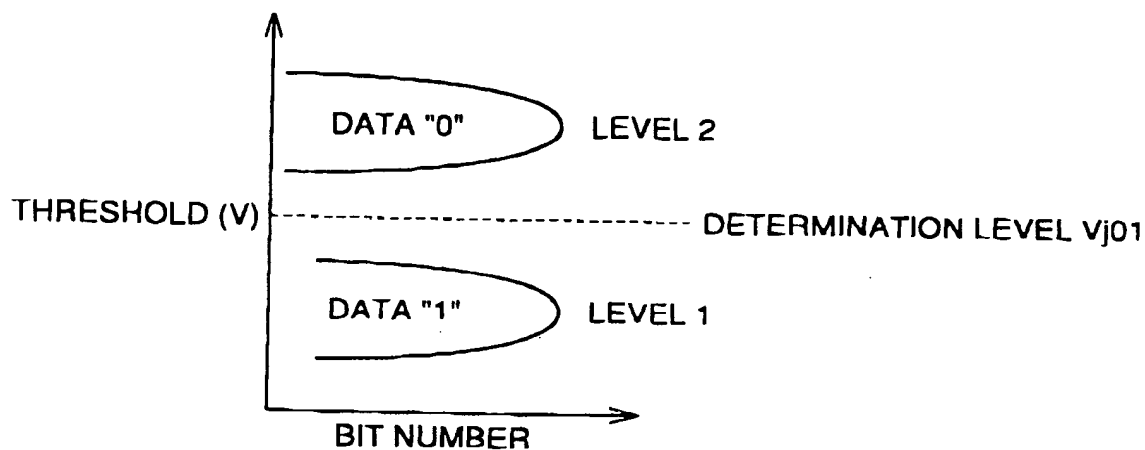


FIG. 120 PRIOR ART

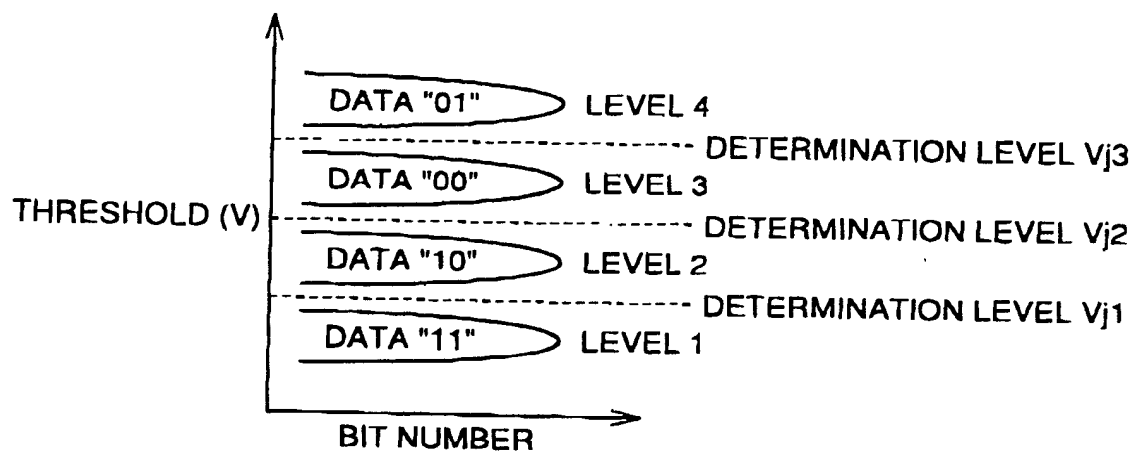


FIG. 121 PRIOR ART

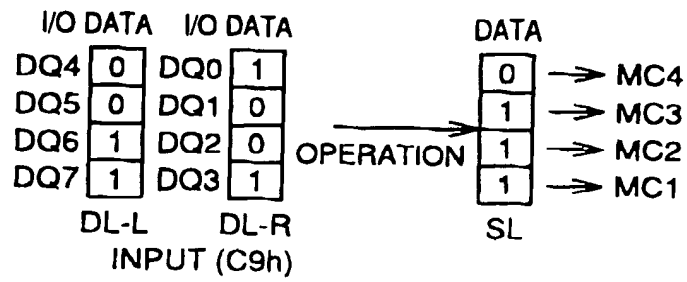


FIG. 122 PRIOR ART

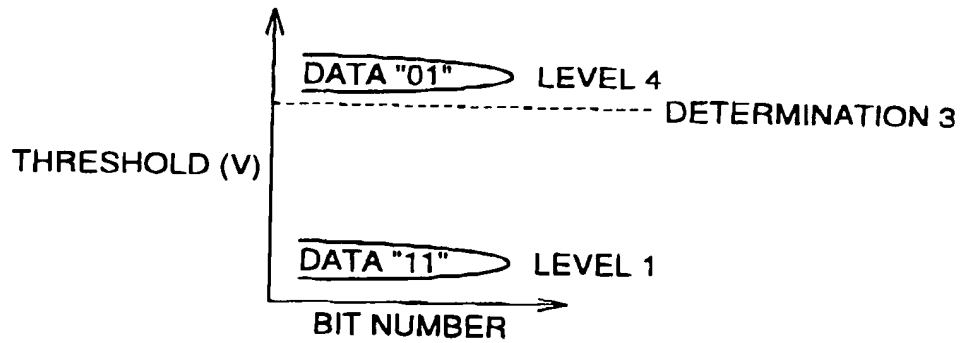


FIG. 123 PRIOR ART

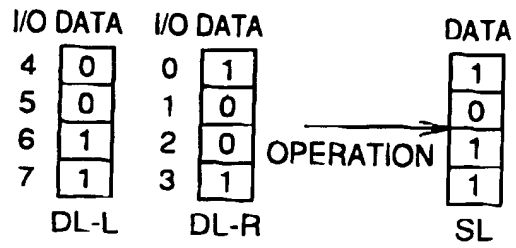
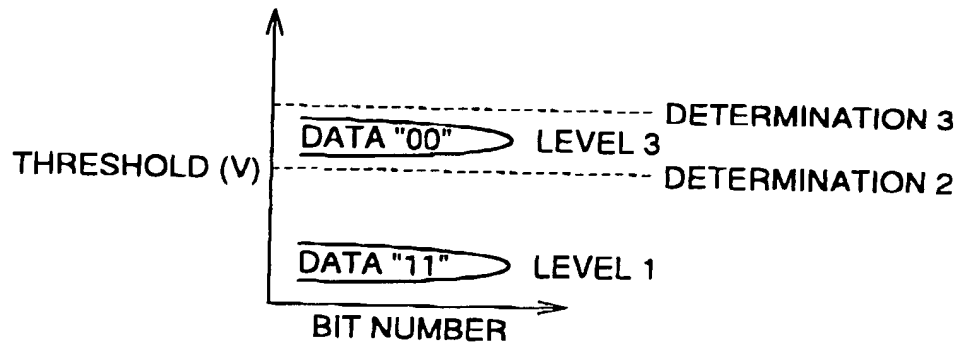
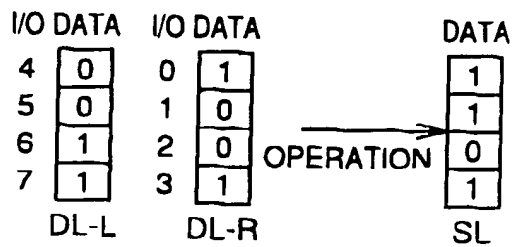


FIG. 124 PRIOR ART



65227-465959

**FIG. 125** PRIOR ART



**FIG. 126** PRIOR ART

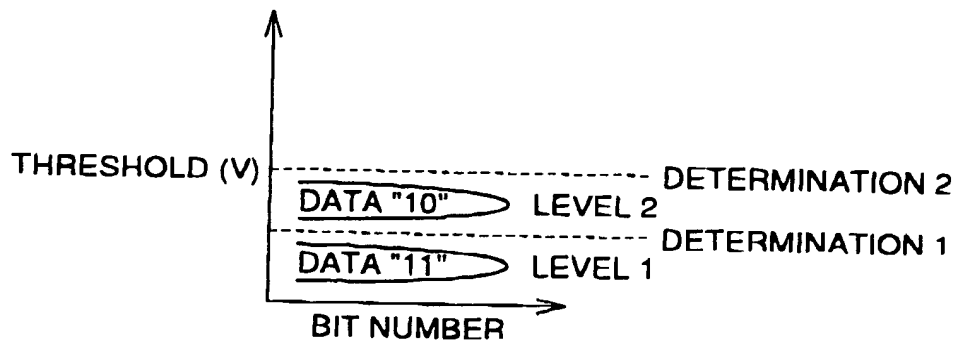


FIG.127 PRIOR ART

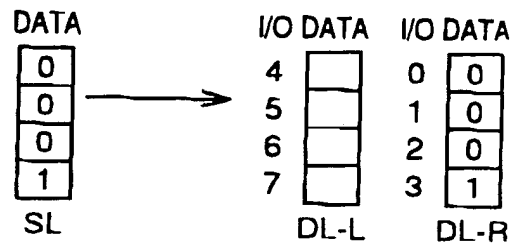


FIG.128 PRIOR ART

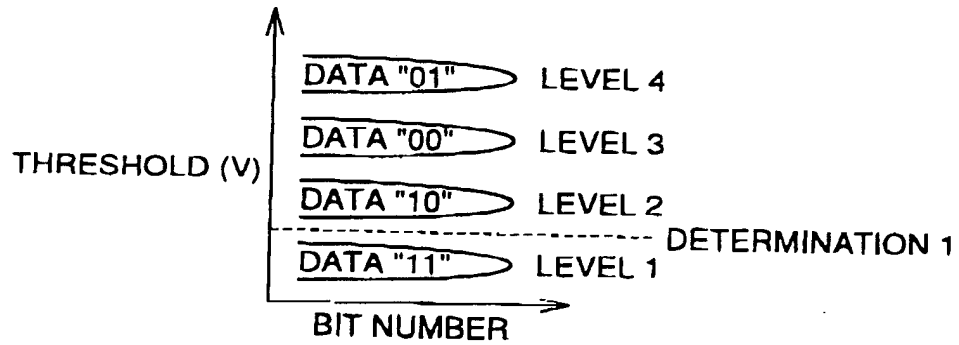


FIG. 129 PRIOR ART

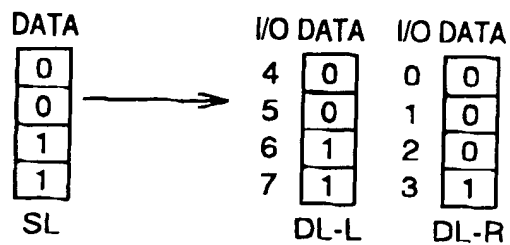


FIG. 130 PRIOR ART

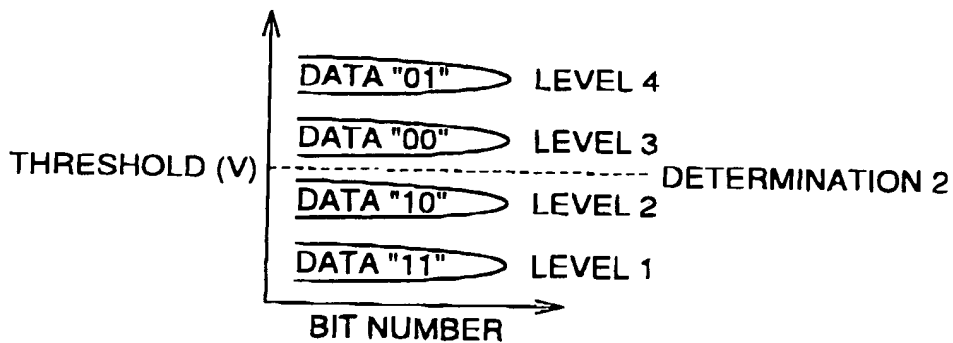


FIG. 131 PRIOR ART

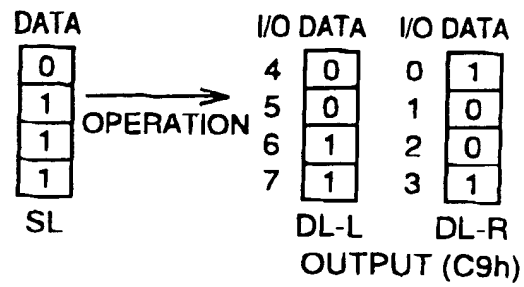


FIG. 132 PRIOR ART

